MOTOROLA

MC13142

Product Preview

Low Power DC – 1.8 GHz LNA, Mixer and VCO

The MC13142 is intended to be used as a first amplifier, voltage controlled oscillator and down converter for RF applications. It features wide band operation, low noise, high gain and high linearity while maintaining low current consumption. The circuit consists of a Low Noise Amplifier (LNA), a Voltage Controlled Oscillator (VCO), a buffered oscillator output, a mixer, an Intermediate Frequency amplifier (IF_{amp}) and a dc control section. The wide mixer IF bandwidth allows this part also to be used as an up converter and exciter amplifier.

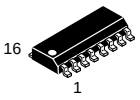
- Wide RF Bandwidth: DC–1.8 GHz
- Wide LO Bandwidth: DC–1.8 GHz
- Wide IF Bandwidth: DC–1.8 GHz
- Low Power: 13 mA @ V_{CC} = 2.7–6.5 V
- High Mixer Linearity: $P_{i1.0\ dB}$ = +3.0 dBm
- Linearity Adjustment Increases IP_{3in} Up to +20 dBm
- Single–Ended 50 Ω Mixer Input
- Double Balanced Mixer Operation
- Open Collector Mixer Output
- Single Transistor Oscillator with Collector, Base and Emitter Pinned Out
- Buffered Oscillator Output
- Mixer and Oscillator Can be Enabled Independently in TQFP–20 Package Only

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13142D	T_A = –40° to +85°C	SO–16
MC13142FTB		TQFP–20

LOW POWER DC – 1.8 GHz LNA, MIXER and VCO

SEMICONDUCTOR TECHNICAL DATA

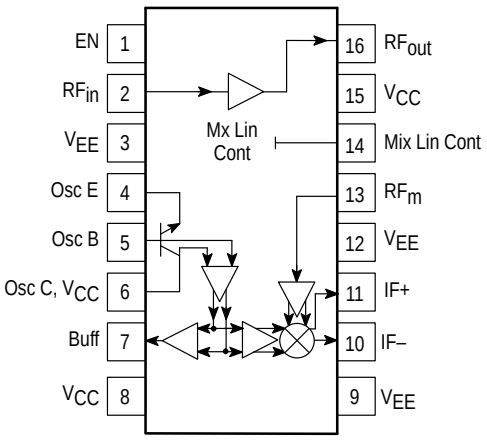


D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

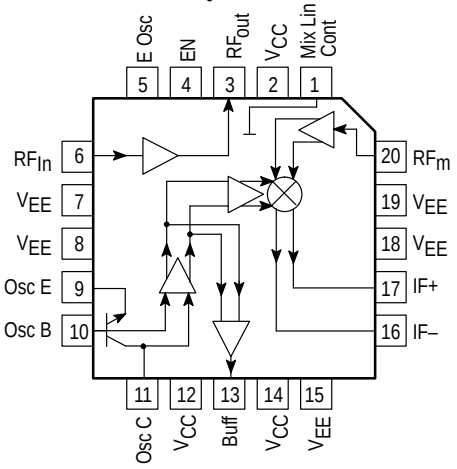
FTB SUFFIX
PLASTIC PACKAGE
CASE 976
(Thin QFP)

PIN CONNECTIONS

SO–16



TQFP–20



This device contains 176 active transistors.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0 (max)	Vdc
Operating Supply Voltage Range	V_{CC}	2.7–6.5	Vdc

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.0 V, T_A = 25°C, LO_{in} = –10 dBm @ 950 MHz, IF @ 50 MHz.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (Power Down)	I_{CC}	–	100	–	pA
Supply Current (Power Up)	I_{CC}	–	13.5	–	mA
Amplifier Gain (50 Ω Insertion Gain)	S_{21}	–	12	–	dB
Amplifier Reverse Isolation	S_{12}	–	–33	–	dB
Amplifier Input Match	$\Gamma_{in\ amp}$	–	–10	–	dB
Amplifier Output Match	$\Gamma_{out\ amp}$	–	–15	–	dB
Amplifier 1.0 dB Gain Compression	$Pin_{-1.0\ dB}$	–	–15	–	dBm
Amplifier Input Third Order Intercept	$IP3_{in}$	–	–5.0	–	dBm
Amplifier Noise Figure (Application Circuit)	NF	–	1.8	–	dB
Amplifier Gain @ N.F.	G_{NF}	–	17	–	dB
Mixer Voltage Conversion Gain (R_P = R_L = 800 Ω)	VG_C	–	9.0	–	dB
Mixer Power Conversion Gain (R_P = R_L = 800 Ω)	PG_C	–	–3.0	–	dB
Mixer Input Match	$\Gamma_{in\ M}$	–	–20	–	dB
Mixer SSB Noise Figure	NF_{SSBM}	–	12	–	dB
Mixer 1.0 dB Gain Compression	$Pin_{-1.0\ dBM}$	–	3.0	–	dBm
Mixer Input Third Order Intercept	$IP3_{InM}$	–	–1.0	–	dBm
Oscillator Buffer Drive (50 Ω)	P_{VCO}	–	–16	–	dBm
Oscillator Phase Noise @ 25 kHz Offset	N_Φ	–	–90	–	dBc/Hz
RF_{in} Feedthrough to RF_m	$P_{RFin–RFm}$	–	–35	–	dB
RF_{out} Feedthrough to RF_m	$P_{RFout–RFm}$	–	–35	–	dB
LO Feedthrough to IF	$P_{LO–IF}$	–	–35	–	dBm
LO Feedthrough to RF_{in}	$P_{LO–RFin}$	–	–35	–	dBm
LO Feedthrough to RF_m	$P_{LO–RFm}$	–	–35	–	dBm
Mixer RF Feedthrough to IF	$P_{RFm–IF}$	–	–25	–	dB
Mixer RF Feedthrough to RF_{in}	$P_{RFm–RFin}$	–	–25	–	dB

CIRCUIT DESCRIPTION

General

The MC13142 is a low power LNA, double–balanced Mixer, and VCO. This device is designated for use as the frontend section in analog and digital FM systems such as Digital European Cordless Telephone (DECT), PHS, PCS, Cellular, UHF and 800 MHz Special Mobile Radio (SMR), UHF Family Radio Services and 902 to 928 MHz cordless telephones. It features a mixer linearity control to preset or auto program the mixer dynamic range, an enable function and a wideband IF so the IC may be used either as a down converter or an up converter. Further details are covered in the Pin by Pin Description which shows the equivalent internal circuit and external circuit requirements.

Current Regulation/Enable

Temperature compensating voltage independent current regulators are controlled by the enable function in which “high” powers up the IC.

Low Noise Amplifier (LNA)

The LNA is internally biased at low supply current (approximately 2.0 mA emitter current) for optimal noise figure and gain. The LNA output is biased internally with a 600 Ω resistor to V_{CC}. Input and output matching may be achieved at various frequencies using few external components. Matching the LNA for Maximum stable gain (MSG) yields noise performance within a few tenths of a dB of the minimum noise figure.

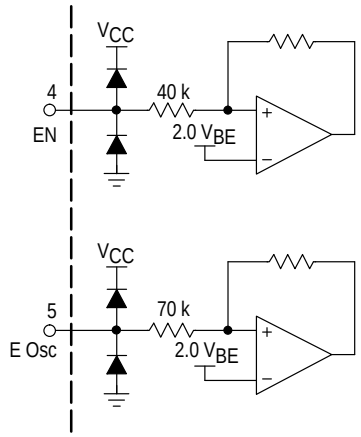
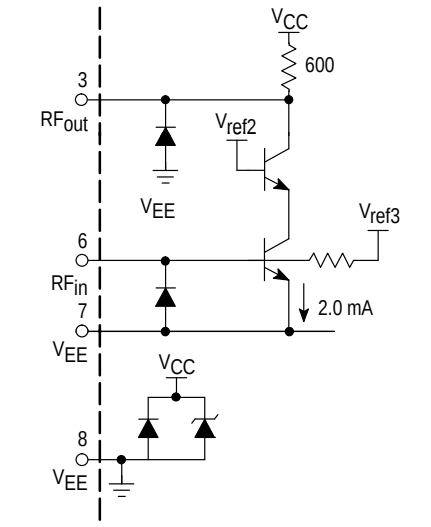
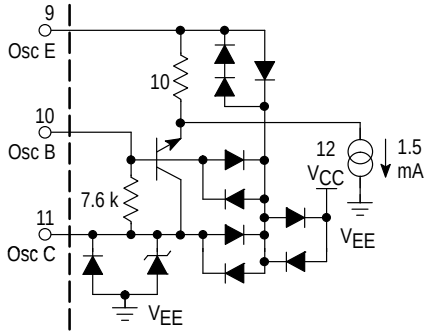
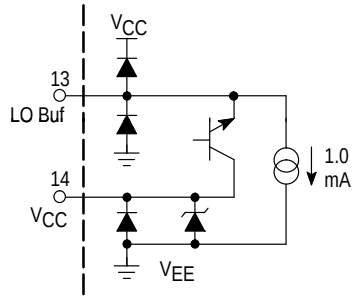
Mixer

The mixer is a double–balanced four quadrant multiplier biased class AB allowing for programmable linearity control via an external current source. An input third order intercept point of 20 dBm may be achieved. All 3 ports of the mixer are designed to work up to 1.8 GHz. The mixer has a 50 Ω single–ended RF input and open collector differential IF outputs. An on–board Local Oscillator transistor has the emitter, base and collector pinned out to implement a low phase noise VCO in various configurations. Additionally, a buffered LO output is provided for operation with a frequency synthesizer. The linear gain of the mixer is approximately 0 dB with a SSB noise figure of 12 dB in the IF output circuit configuration shown in the application example.

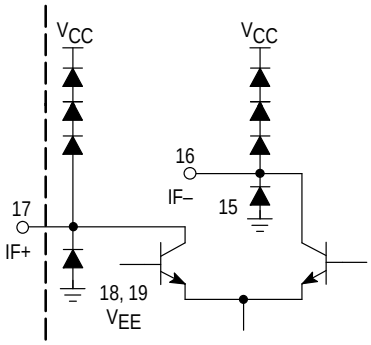
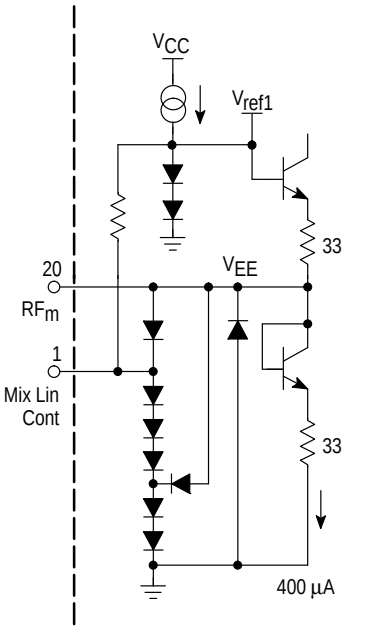
Local Oscillator

The on–chip transistor operates with coaxial transmission line or LC resonant elements to over 2.0 GHz. Biasing is done with a temperature compensated current source in the emitter and a collector to base internal resistor of 7.6 kΩ; however, an RFC from V_{CC} to base is recommended. The application circuit shows a voltage controlled Clapp oscillator operating at center frequency of 975 MHz.

PIN FUNCTION DESCRIPTION

Pin		Symbol	Equivalent Internal Circuit (20 Pin TQFP)	Description
16 Pin SOIC	20 Pin TQFP			
1	4 5	EN E Osc		**Enable, E Osc** In SO–16, both enables, (for the Oscillator/LO Buffer and LNA/Mixer) are bonded to Pin 1. In the TQFP, two pins are provided, Pin 5, E Osc enables the oscillator and buffer while Pin 4, EN enables the LNA/Mixer. Enable by pulling up to V_{CC} or to greater than 2.0 V_{BE}.
2	6	RF_{in}		**RF Input** The input is the base of an NPN low noise amplifier. Minimum external matching is required to optimize the input return loss and gain.
3	7, 8	V_{EE}		**V_{EE} – Negative Supply** V_{EE} pin is taken to an ample dc ground plane through a low impedance path. The path should be kept as short as possible. A two sided PCB is implemented so that ground returns can be easily made through via holes.
16	3	RF_{out}		**RF Output** The output is from the collector of the LNA; it is internally biased with a 600 Ω resistor to V_{CC}. As shown in the 926 MHz application receiver the output is conjugately matched with a shunt L, and series L and C network.
4 5 6	9 10 11	Osc E Osc B Osc C		**On–Board VCO Transistor** The transistor has the emitter, base and collector + V_{CC} pins available. Internal biasing which is compensated for stability over temperature is provided. It is recommended that the base pin is pulled up to V_{CC} through an RFC chosen for the particular oscillator center frequency. The application circuit shows a modified Colpitts or Clapp oscillator configuration and its design is discussed in detail in the application section.
6 8	12 14	V_{CC} V_{CC}		**Supply Voltage (V_{CC})** Two V_{CC} pins are provided for the Local Oscillator and LO Buffer Amplifier. The operating supply voltage range is from 2.7 Vdc to 6.5 Vdc. In the PCB layout, the V_{CC} trace must be kept as wide as feasible to minimize inductive reactances along the trace. V_{CC} should be decoupled to V_{EE} at the IC pin as shown in the component placement view.
7	13	LO Buff		**Local Oscillator Buffer** This is a buffered output providing –16 dBm (50 Ω termination) to drive the f_{in} pin of a PLL synthesizer. Impedance matching to the synthesizer may be necessary to deliver the optimal signal and to improve the phase noise performance of the VCO.

PIN FUNCTION DESCRIPTION (continued)

Pin		Symbol	Equivalent Internal Circuit (20 Pin TQFP)	Description
16 Pin SOIC	20 Pin TQFP			
9, 12	15, 18, 19	V_{EE}		**V_{EE}, Negative Supply** These pins are V_{EE} supply for the mixer IF output. In the application PC board these pins are tied to a common V_{EE} trace with other V_{EE} pins.
10, 11	16, 17	IF–, IF+		**IF Output** The IF is a differential open collector configuration which designed to use over a wide frequency range for up conversion as well as down conversion. Differential to single–ended circuit configuration and matching options are discussed in the application section. 6.0 dB of additional Mixer gain can be achieved by conjugately matching at the desired IF frequency.
13	20	RF_m		**Mixer RF Input** The mixer input impedance is broadband 50 Ω for applications up to 1.8 GHz. It easily interfaces with a RF ceramic filter as shown in the application schematic.
14	1	Mix Lin Cont		**Mixer Linearity Control** The mixer linearity control circuit accepts approximately 0 to 2.3 mA control current to set the dynamic range of the mixer. An Input Third Order Intercept Point, IIP3 of 20 dBm may be achieved at 2.3 mA of control current (approximately 7.0 mA of additional supply current).

APPLICATIONS INFORMATION

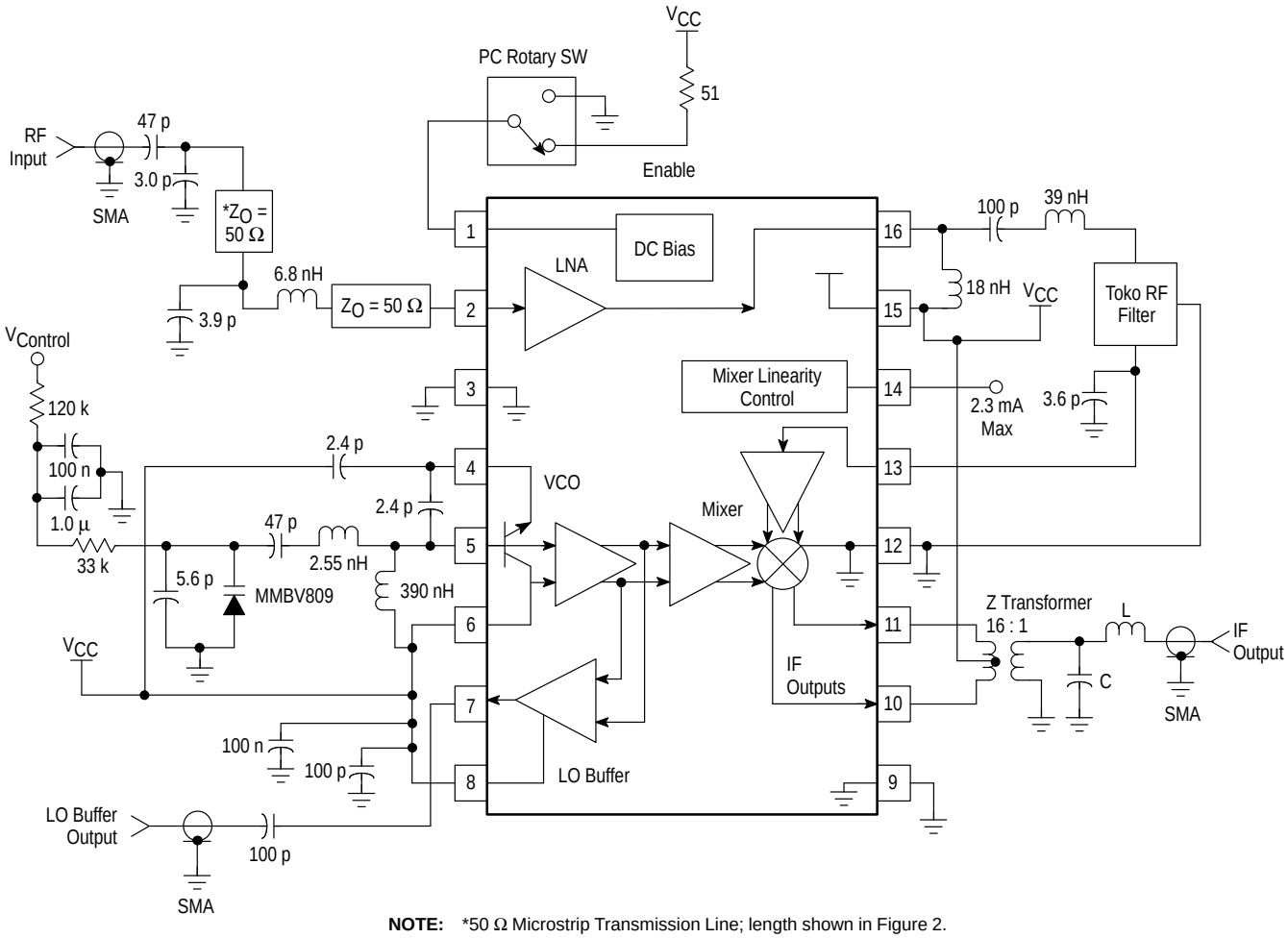
Evaluation PC Board

The evaluation PCB is very versatile and is intended to be used across the entire useful frequency range of this device. The PC board accommodates all SMT components on the circuit side (see Circuit Side Component Placement View). This evaluation board will be discussed and referenced in this section.

Component Selection

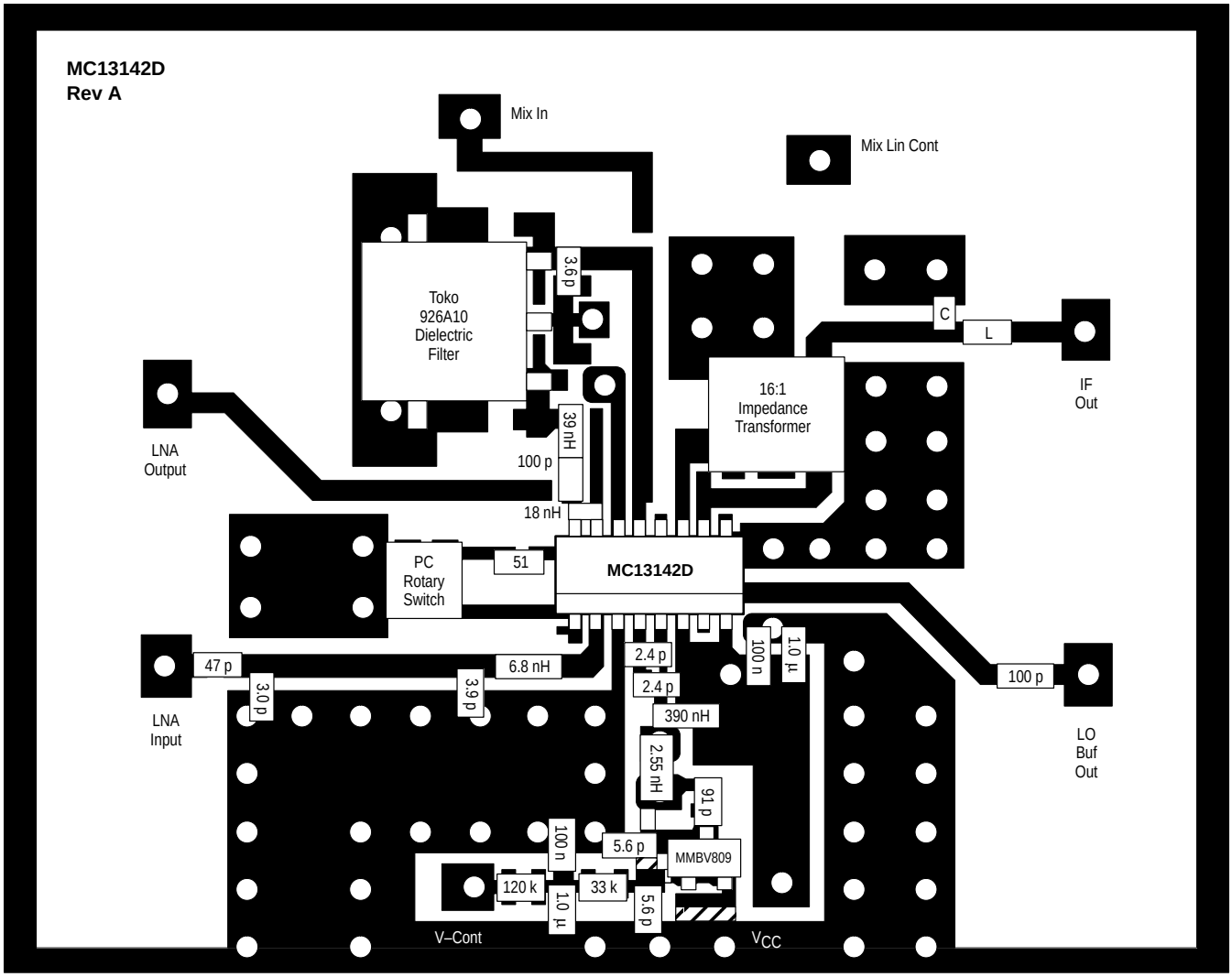
The evaluation PC board is designed to accommodate specific components, while also being versatile enough to use components from various manufacturers. The circuit side placement view is illustrated for the components specified in the application circuit. The application circuit schematic specifies particular components that were used to achieve the results given and specified in the tables but alternate components of the same Q and value should give equivalent results.

Figure 1. Application Circuit
(926.5 MHz)



NOTE: *50 Ω Microstrip Transmission Line; length shown in Figure 2.

Figure 2. Circuit Side Component Placement View



NOTES: The PCB is laidout for the 4DFA (2 pole SMD type) and 4DFB (3 pole SMD type) filters which are available for applications in cellular and GSM,GPS (1.2–1.5 GHz), DECT, PHS and PCS (1.8–2.0 GHz) and ISM Bands (902–928 MHz and 2.4–2.5 GHz). In the component placement shown above, the 926.5 MHz dielectric type image filter is used (Toko Part # 4DFA–926A10).

The PCB also accommodates a surface mount SAW filter in an eight or six pin ceramic package for the cellular base and handset frequencies. Recommended manufacturers are Siemens and Murata.

Traces are provided on the PCB to evaluate the LNA and mixer separately. The component placement view shows external circuit components used for the 926.5 MHz application circuit. Note: some traces must be cut to accommodate placement of components; likewise some traces must be shorted. The voltage controlled oscillator is shown with the varactor referenced to V_{EE} ground. The PCB is modified as shown to do this.

16:1 broadband impedance transformer is mini circuits part #TX16–R3T; it is in the leadless surface mount “TX” package. Components L and C comprise a low pass filter used to provide narrowband matching at a given IF frequency. For example at 49 MHz C = 36 p and L = 330 nH.
The microstrip trace on the ground side of the PCB is intended for a microstrip resonator; it is cut free when using a lump inductor as done above.

Input Matching/Components

It is desirable to use a RF ceramic or SAW filter before the mixer to provide image frequency rejection. The filter is selected based on cost, size and performance tradeoffs. Typical RF filters have 3.0 to 5.0 dB insertion loss. The PC board layout accommodates both ceramic and SAW RF filters which are offered by various suppliers such as Siemens, Toko and Murata.

Interface matching between the LNA, RF filter and the mixer will be required. The interface matching networks shown in the application circuit are designed for 50 Ω interfaces.

In the application circuit, the LNA is conjugately matched to 50 Ω input and output for 3.0 to 5.0 Vdc V_{CC}. 17 dB gain and 1.8 dB noise figure is typical at 926 MHz. The mixer measures 0 dB gain and 12 dB noise figure as shown in the application circuit. Typical insertion loss of the Toko ceramic filter is 3.0 dB. Thus, the overall gain of the frontend receiver is 14 dB with a 3.3 dB noise figure.

System Noise Considerations

The block diagram shows the cascaded noise stages of the MC13142 in the frontend receiver subsystem; it represents the application circuit. In the cascaded noise analysis the system noise equation is:

Fsystem = F1 + [(F2 –1)/G1] + [(F3–1)]/[(G1)(G2)]

where:

F1 = the Noise Factor of the MC13142 LNA
G1 = the Gain of the LNA
F2 = the Noise factor of the RF Ceramic Filter
G2 = the Gain of the Ceramic Filter
F3 = the Noise factor of the Mixer

Note: the above terms are defined as linear relationships and are related to the log form for gain and noise figure by the following:

F = Log $^{-1}$ [(NF in dB)/10] and similarly
G = Log $^{-1}$ [(Gain in dB)/10].

Calculating in terms of gain and noise factor yields the following:

F1 = 1.51; G1 = 50.11
F2 = 1.99; G2 = 0.5
F3 = 15.85

Thus, substituting in the equation for system noise factor:

Fsystem = 2.12; NFsystem = 3.3 dB

Figure 3. Frontend Subsystem Block Diagram for Noise Analysis

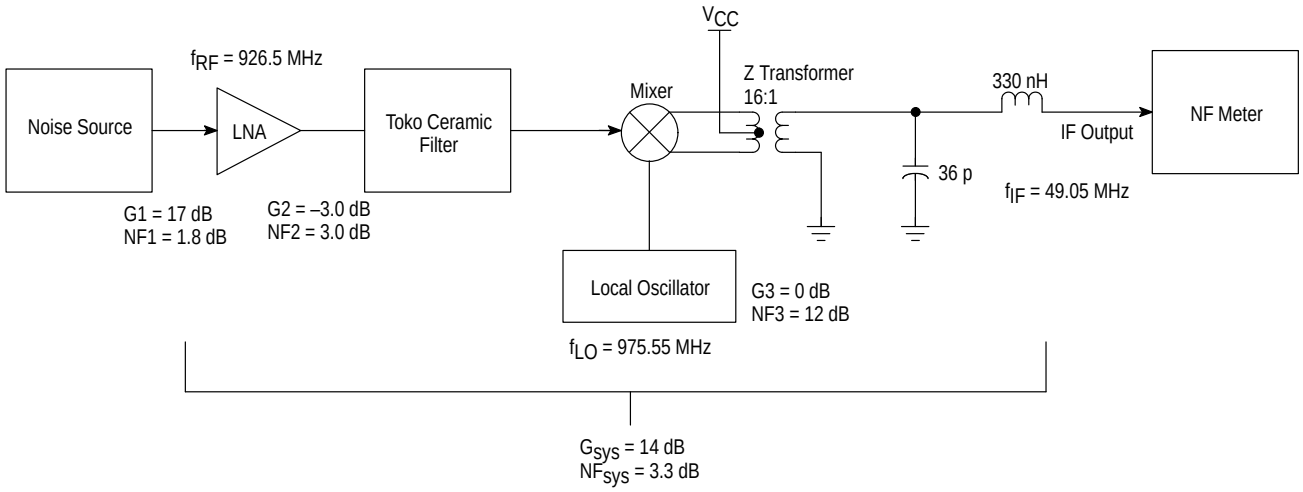
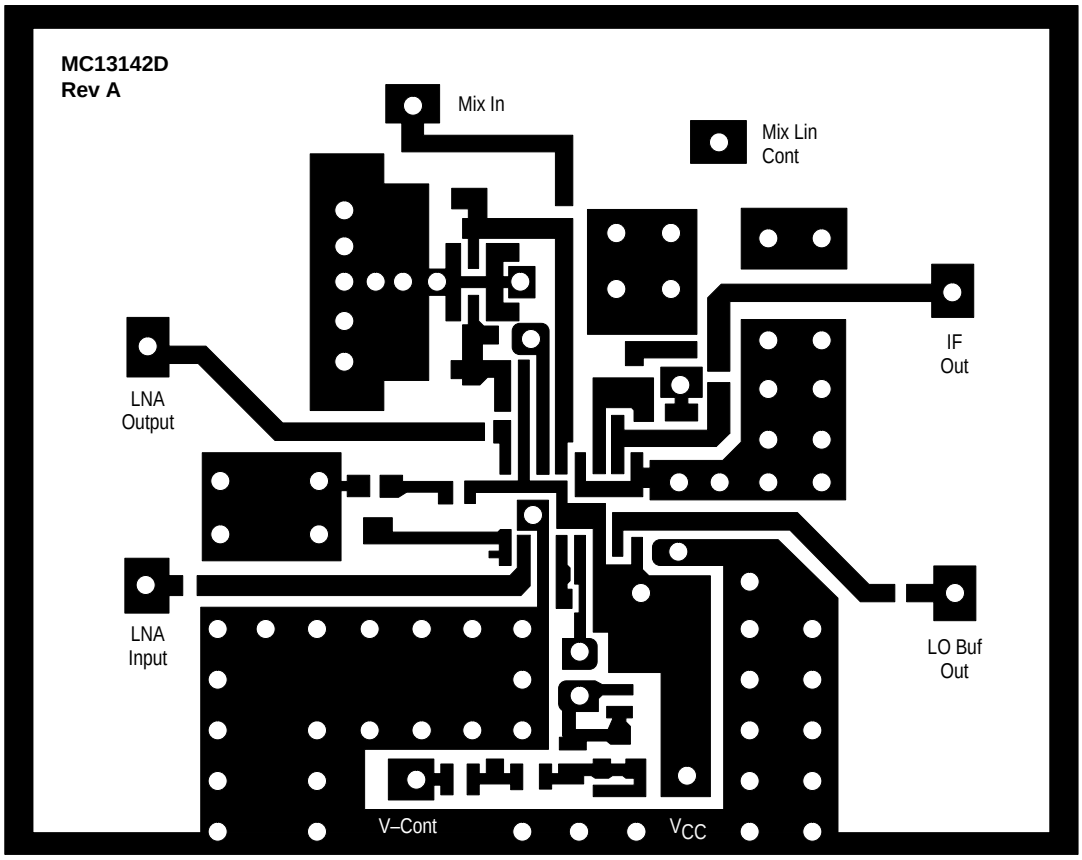
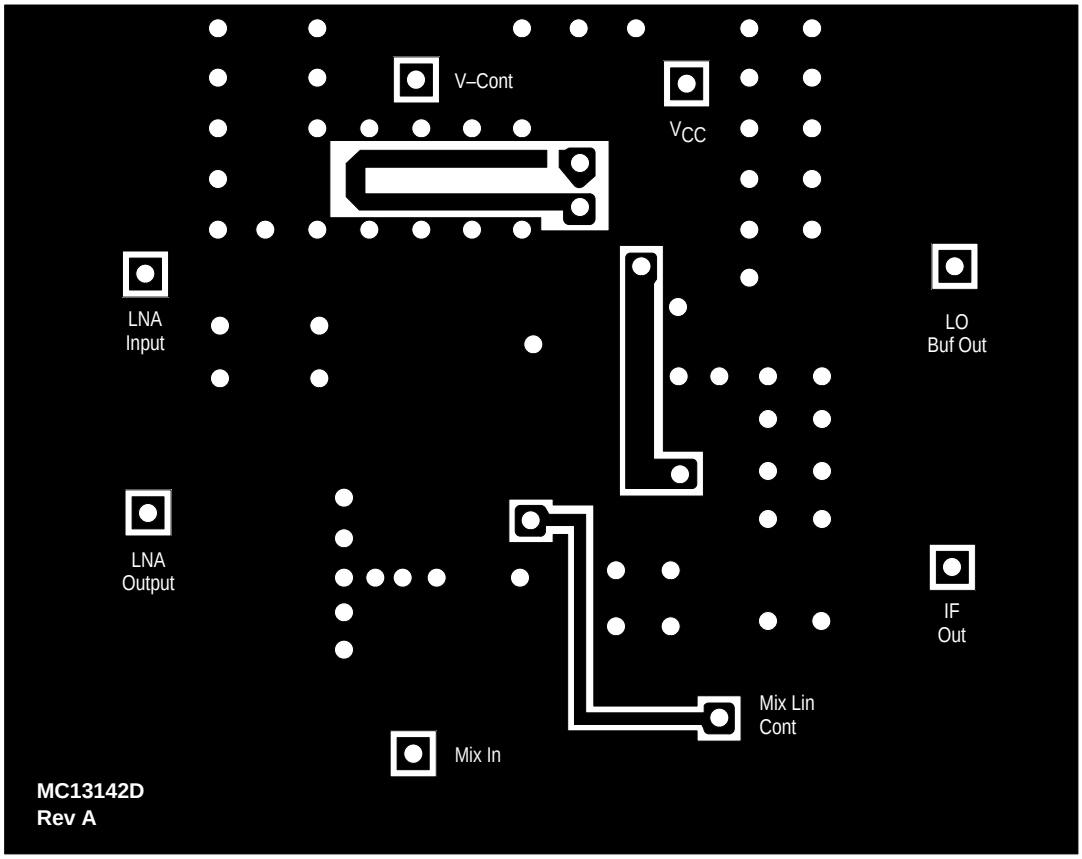


Figure 4. Circuit Side View



NOTES: Critical dimensions are 50 mil centers lead to lead in SO–16 footprint.
Also line widths to labeled ports excluding V_{CC} are 50 mil (0.050 inch).
FR4 PCB, 1/32 inch.

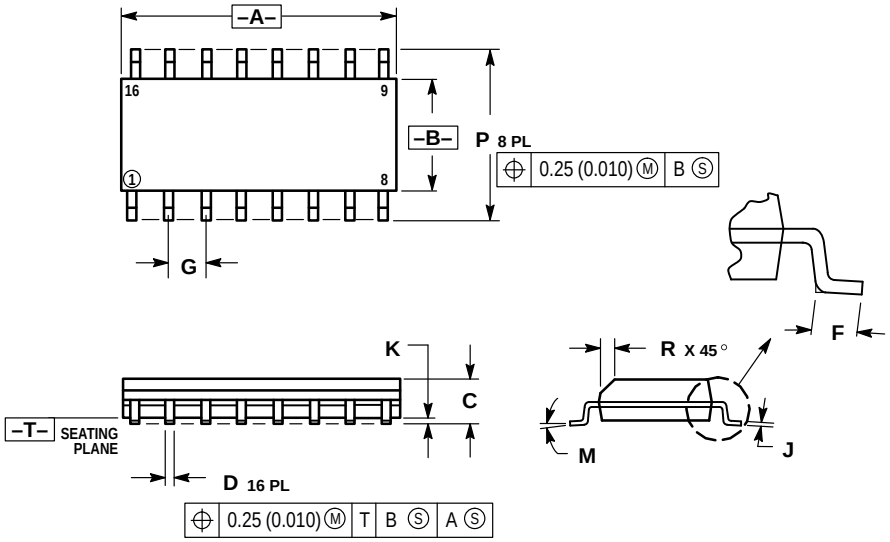
Figure 5. Ground Side View



NOTES: FR4 PCB, 1/32 inch.

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC PACKAGE
CASE 751B–05
(SO–16)
ISSUE J

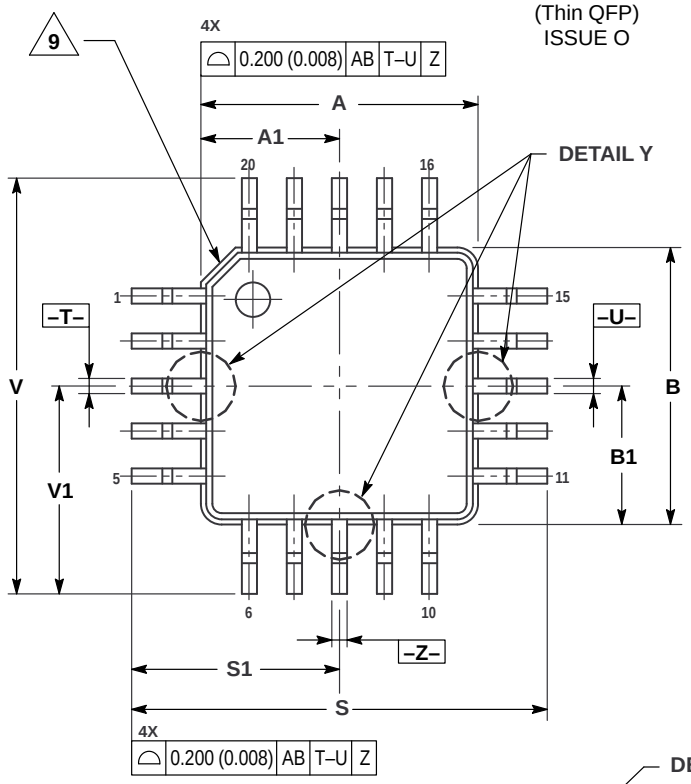


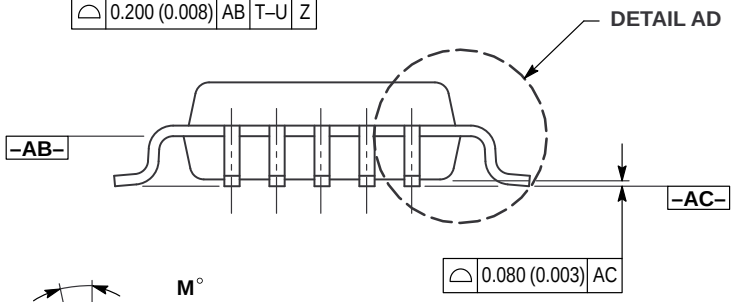
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

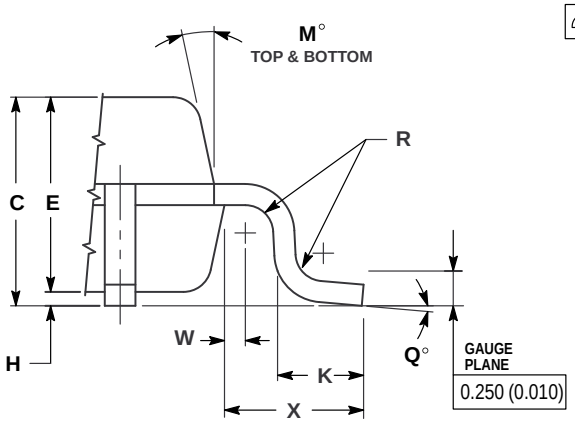
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

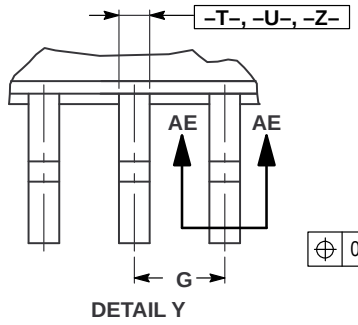
OUTLINE DIMENSIONS

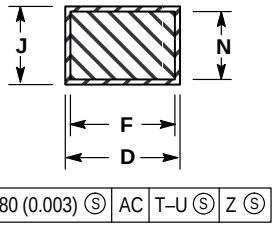
FTB SUFFIX
PLASTIC PACKAGE
CASE 976–01
(Thin QFP)
ISSUE O











NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT DATUM PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350 (0.014).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.000 BSC		0.157 BSC	
A1	2.000 BSC		0.079 BSC	
B	4.000 BSC		0.157 BSC	
B1	2.000 BSC		0.079 BSC	
C	1.400	1.600	0.055	0.063
D	0.170	0.270	0.007	0.011
E	1.350	1.450	0.053	0.057
F	0.170	0.230	0.007	0.009
G	0.650 BSC		0.026 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.250 BSC		0.010 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	6.000 BSC		0.236 BSC	
S1	3.000 BSC		0.118 BSC	
V	6.000 BSC		0.236 BSC	
V1	3.000 BSC		0.118 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

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MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298