EM78P153S

8-BIT MICRO-CONTROLLER

Version 1.4

Specification Revision History		
Version	**Content**	
1.1	*Initial version*	
1.2	*Change Initialized Register Values, Internal RC Drift Rate, DC and AC Electrical Characteristic*	*05/02/2003*
1.3	*Change Power on reset content*	*06/25/2003*
1.4	*Add the Device Characteristic at section 6.3*	*12/31/2003*

Application Note

AN-001 Q & A on ICE153S

AN-002 The Set-up Timing and Pin Change Wake-up Function Application

AN-003 Internal RC Oscillator Mode

1. GENERAL DESCRIPTION

EM78P153S is an 8-bit microprocessor with low-power and high-speed CMOS technology. It is equipped with a 1024*13-bits Electrical One Time Programmable Read Only Memory (OTP-ROM) within it. It provides a PROTECTION bit to prevent intrusion of user's code in the OTP memory as well as 15 OPTION bits to match user's requirements.

With its OTP-ROM feature, the EM78P153S offers users a convenient way of developing and verifying their programs. Moreover, user developed code can be easily programmed with the ELAN writer.

2. FEATURES

- 14-lead packages : EM78P153S
- Operating voltage range : 2.3V~5.5V
- Available in temperature range: 0°C~70°C
- Operating frequency range (base on 2 clocks):
    * Crystal mode: DC~20MHz at 5V, DC~8MHz at 3V, DC~4MHz at 2.3V.
    * ERC mode: DC~4MHz at 5V, DC~4MHz at 3V, DC~4MHz at 2.3V.
- Low power consumption:
    * less then 1.5 mA at 5V/4MHz
    * typical of 15 μA, at 3V/32KHz
    * typical of 1μA, during the sleep mode
- 1024 × 13 bits on chip ROM
- Built-in calibrated IRC oscillators (8MHz, 4MHz, 1MHz, 455KHz)
- Programmable prescaler of oscillator set-up time
- One security register to prevent the code in the OTP memory from intruding
- One configuration register to match the user's requirements
- 32× 8 bits on chip registers (SRAM, general purpose register)
- 2 bi-directional I/O ports
- 5 level stacks for subroutine nesting
- 8-bit real time clock/counter (TCC) with selective signal sources and trigger edges, and with overflow interrupt
- Power down mode (SLEEP mode)
- Three available interruptions
    * TCC overflow interrupt
    * Input-port status changed interrupt (wake up from the sleep mode)
    * External interrupt
- Programmable free running watchdog timer
- 7 programmable pull-high I/O pins
- 7 programmable open-drain I/O pins
- 6 programmable pull-down I/O pins
- Two clocks per instruction cycle
- Package type: 14 pins SOP, DIP
    * 14 pin DIP 300mil: EM78P153SP

* 14 pin SOP 150mil: EM78P153SN

• The transient point of system frequency between HXT and LXT is around 400KHz.

3. PIN ASSIGNMENTS

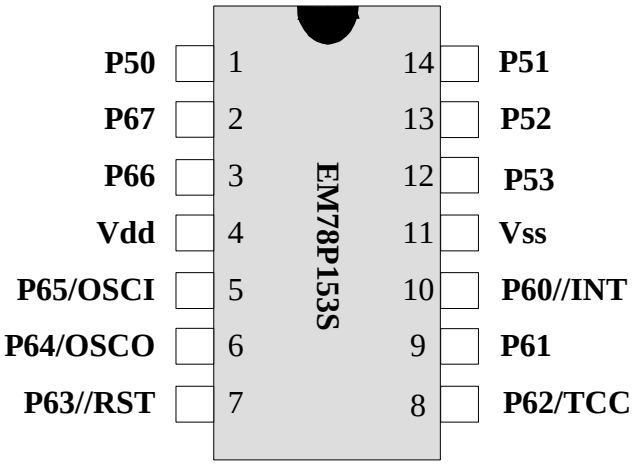


Fig. 1 Pin assignment

Table 1 Pin description

Symbol	Pin No.	Type	Function
Vdd	4	-	Power supply.
P65/OSCI	5	I/O	* General purpose I/O pin. * External clock signal input. * Input pin of XT oscillator. * Pull-high/open-drain * Wake up from sleep mode when the status of the pin changes.
P64/OSCO	6	I/O	* General purpose I/O pin. * External clock signal input. * Input pin of XT oscillator. * Pull-high/open-drain * Wake up from sleep mode when the status of the pin changes.
P63//RESET	7	I	* If set as /RESET and remain at logic low, the device will be under reset. * Wake up from sleep mode when the status of the pin changes. * Voltage on /RESET must not exceed Vdd during the normal mode. * Internal Pull-high is on if defined as /RESET. * P63 is input pin only
P62/TCC	8	I/O	* General purpose I/O pin. * Pull-high/open-drain/pull-down. * Wake up from sleep mode when the status of the pin changes. * External Timer/Counter input.
P61	9	I/O	* General purpose I/O pin. * Pull-high/open-drain/pull-down. * Wake up from sleep mode when the status of the pin changes. * Schmitt Trigger input during the programming mode
P60//INT	10	I/O	* General purpose I/O pin. * Pull-high/open-drain/pull-down. * Wake up from sleep mode when the status of the pin changes. * Schmitt Trigger input during the programming mode.

			* External interrupt pin triggered by falling edge.
P66, P67	2, 3	I/O	* General purpose I/O pin. * Pull-high/open-drain. * Wake up from sleep mode when the status of the pin changes.
P50~P53	1,14~13	I/O	* General purpose I/O pin. * Pull-down
P53	12	I/O	* General purpose I/O pin.
VSS	11	-	*Ground.

4. FUNCTION DESCRIPTION

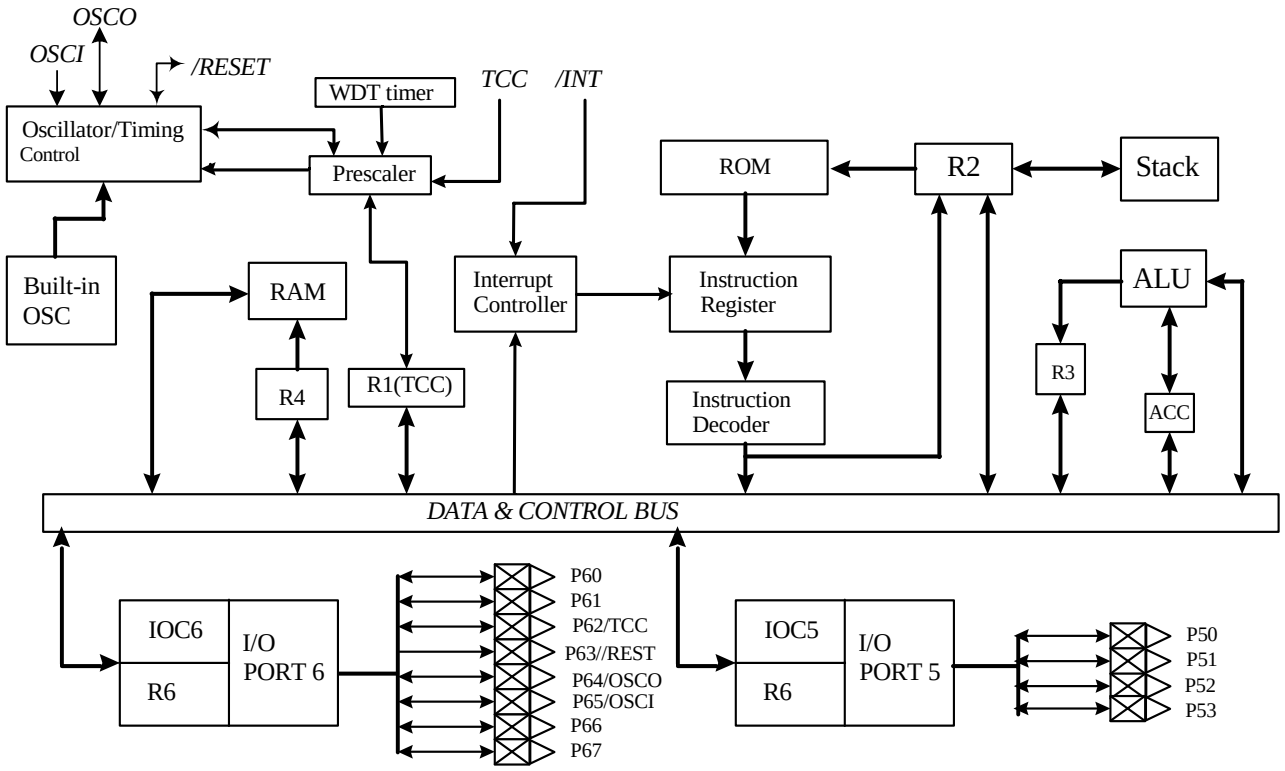


Fig. 2 Functional block diagram

4.1 Operational Registers

1. R0 (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is to be an indirect addressing pointer. Any instruction using R0 as a pointer, actually accesses data pointed by the RAM Select Register (R4).

2. R1 (Time Clock /Counter)

- Increased by an external signal edge, which is defined by TE bit (CONT-4) through the TCC pin, or by the instruction cycle clock.
- Writable and readable as any other registers.
- Defined by resetting PAB (CONT-3).
- The prescaler is assigned to TCC if the PAB bit (CONT-3) is reset.
- The contents of the prescaler counter is cleared only when a value is written to TCC register.

3. R2 (Program Counter) & Stack

- Depending on the device type, R2 and hardware stack are 10-bit wide. The structure is depicted in Fig.3.
- 1024×13 bits on-chip OTP ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- R2 is set as all "0"s when at RESET condition.
- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows PC to go to any location within a page.
- "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.
- "ADD R2,A" allows the contents of 'A' to be added to the current PC, and the ninth and tenth bits of the PC are cleared.
- "MOV R2,A" allows to load an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits of the PC are cleared.
- Any instruction that is written to R2 (e.g. "ADD R2,A", "MOV R2,A", "BC R2,6",·····) will cause the ninth and tenth bits (A8,A9) of the PC to be cleared. Thus, the computed jump is limited to the first 256 locations of a page.
- All instructions are single instruction cycle (fclk/2 or fclk/4), except for the instruction that would change the contents of R2. This instruction will need one more instruction cycle.

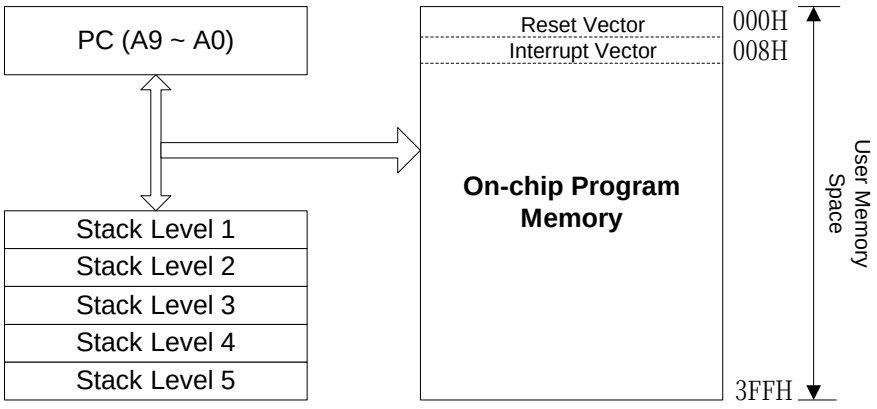


Fig. 3 Program counter organization

Address	R PAGE registers	IOC PAGE registers
00	**R0**	Reserve
01	**R1** (TCC)	**CONT** (Control Register)
02	**R2** (PC)	Reserve
03	**R3** (Status)	Reserve
04	**R4** (RSR)	Reserve
05	**R5** (Port5)	**IOC5** (I/O Port Control Register)
06	**R6** (Port6)	**IOC6** (I/O Port Control Register)
07	Reserve	Reserve
08	Reserve	Reserve
09	Reserve	Reserve
0A	Reserve	Reserve
0B	Reserve	**IOCB** (Pull-down Register)
0C	Reserve	**IOCC** (Open-drain Control)
0D	Reserve	**IOCD** (Pull-high Control Register)
0E	Reserve	**IOCE** (WDT Control Register)
0F	**RF** (Interrupt Status)	**IOCF** (Interrupt Mask Register)
10 : 2F	General Registers	

Fig. 4 Data memory configuration

4. R3 (Status Register)

7	6	5	4	3	2	1	0
RST	GP1	GP0	T	P	Z	DC	C

• **Bit 7 (RST)** Bit for reset type.

Set to 1 if wake-up from sleep mode on pin change

Set to 0 if wake up from other reset types

• **Bit6 ~ 5 (GP1 ~ 0)** General purpose read/write bits.

• **Bit 4 (T)** Time-out bit.

Set to 1 with the "SLEP" and "WDTC" command, or during power up and reset to 0 by WDT time-out.

• **Bit 3 (P)** Power down bit.

Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

• **Bit 2 (Z)** Zero flag.

Set to "1" if the result of an arithmetic or logic operation is zero.

• **Bit 1 (DC)** Auxiliary carry flag

• **Bit 0 (C)** Carry flag

5. R4 (RAM Select Register)

• **Bits 7 ~ 6** are general-purpose read/write bits.

See the configuration of the data memory in Fig. 4.

• **Bits 5 ~ 0** are used to select registers (address: 00~06, 0F~2F) in the indirect addressing mode.

6. R5 ~ R6 (Port 5 ~ Port 6)

• R5 and R6 are I/O registers.

• Only the lower 4 bits of R5 are available.

• The upper 4 bits of R5 are fixed to 0.

• P63 is input only.

7. RF (Interrupt Status Register)

7	6	5	4	3	2	1	0
-	-	-	-	-	EXIF	ICIF	TCIF

“1” means interrupt request, and “0” means no interrupt occurs.

• **Bits 7 ~ 3** Not used.

• **Bit 2 (EXIF)** External interrupt flag. Set by falling edge on /INT pin, reset by software.

• **Bit 1 (ICIF)** Port 6 input status changed interrupt flag. Set when Port 6 input changes, reset by software.

• **Bit 0 (TCIF)** TCC overflowing interrupt flag. Set when TCC overflows, reset by software.

• RF can be cleared by instruction but cannot be set.

• IOCF is the interrupt mask register.

• Note that the result of reading RF is the "logic AND" of RF and IOCF.

8. R10 ~ R2F

• All of these are the 8-bit general-purpose registers.

4.2 Special Purpose Registers

1. A (Accumulator)

• Internal data transfer, or instruction operand holding

• It cannot be addressed.

2. CONT (Control Register)

7	6	5	4	3	2	1	0
-	INT	TS	TE	PAB	PSR2	PSR1	PSR0

• **Bit 7** Not used.

• **Bit 6 (INT)** Interrupt enable flag

0: masked by DISI or hardware interrupt

1: enabled by ENI/RETI instructions

• **Bit 5 (TS)** TCC signal source

0: internal instruction cycle clock, P62 is a bi-directional I/O pin.

1: transition on TCC pin

• **Bit 4 (TE)** TCC signal edge

0: increment if the transition from low to high takes place on TCC pin

1: increment if the transition from high to low takes place on TCC pin

• **Bit 3 (PAB)** Prescaler assignment bit.

0: TCC

1: WDT

• **Bit 2 (PSR2) ~ 0 (PSR0)** TCC/WDT prescaler bits.

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

• CONT register is both readable and writable.

3. IOC5 ~ IOC6 (I/O Port Control Register)

• "1" put the relative I/O pin into high impedance, while "0" defines the relative I/O pin as output.

• Only the lower 4 bits of IOC5 are available to be defined.

• IOC5 and IOC6 registers are both readable and writable.

4. IOCB (Pull-down Control Register)

7	6	5	4	3	2	1	0
-	/PD6	/PD5	/PD4	-	/PD2	/PD1	/PD0

• **Bit 7** Not used.

0: Enable internal pull-down

1: Disable internal pull-down

• **Bit 6 (/PD6)** Control bit used to enable the pull-down of P62 pin.

• **Bit 5 (/PD5)** Control bit is used to enable the pull-down of P61 pin.

• **Bit 4 (/PD4)** Control bit is used to enable the pull-down of P60 pin.

• **Bit 3** Not used

• **Bit 2 (/PD2)** Control bit is used to enable the pull-down of P52 pin.

• **Bit 1 (/PD1)** Control bit is used to enable the pull-down of P51 pin.

• **Bit 0 (/PD0)** Control bit is used to enable the pull-down of P50 pin.

• IOCB Register is both readable and writable.

5. IOCC (Open-drain Control Register)

7	6	5	4	3	2	1	0
OD7	OD6	OD5	OD4	-	OD2	OD1	OD0

• **Bit 7 (OD7)** Control bit is used to enable the open-drain of P67 pin.

0: Disable open-drain output

1: Enable open-drain output

• **Bit 6 (OD6)** Control bit is used to enable the open-drain of P66 pin.

• **Bit 5 (OD5)** Control bit is used to enable the open-drain of P65 pin.

• **Bit 4 (OD4)** Control bit is used to enable the open-drain of P64 pin.

• **Bit 3** Not used.

• **Bit 2 (OD2)** Control bit is used to enable the open-drain of P62 pin.

• **Bit 1 (OD1)** Control bit is used to enable the open-drain of P61 pin.

• **Bit 0 (OD0)** Control bit is used to enable the open-drain of P60 pin.

• IOCC Register is both readable and writable.

6. IOCD (Pull-high Control Register)

7	6	5	4	3	2	1	0
/PH7	/PH6	/PH5	/PH4	-	/PH2	/PH1	/PH0

• **Bit 7 (/PH7)** Control bit is used to enable the pull-high of P67 pin.

0: Enable internal pull-high

1: Disable internal pull-high

• **Bit 6 (/PH6)** Control bit is used to enable the pull-high of P66 pin.

• **Bit 5 (/PH5)** Control bit is used to enable the pull-high of P65 pin.

• **Bit 4 (/PH4)** Control bit is used to enable the pull-high of P64 pin.

• **Bit 3** Not used.

• **Bit 2 (/PH2)** Control bit is used to enable the pull-high of P62 pin.

• **Bit 1 (/PH1)** Control bit is used to enable the pull-high of P61 pin.

• **Bit 0 (/PH0)** Control bit used to enable the pull-high of P60 pin.

• IOCD Register is both readable and writable.

7. IOCE (WDT Control Register)

7	6	5	4	3	2	1	0
WDTE	EIS	-	-	-	-	-	-

• **Bit 7 (WDTE)** Control bit used to enable Watchdog timer.

0: Disable WDT.

1: Enable WDT.

WDTE is both readable and writable.

• **Bit 6 (EIS)** Control bit is used to define the function of P60(/INT) pin.

0: P60, bi-directional I/O pin.

1: /INT, external interrupt pin. In this case, the I/O control bit of P60 (bit 0 of IOC6) must be set to "1". When EIS is "0", the path of /INT is masked. When EIS is "1", the status of /INT pin can also be read by way of reading Port 6 (R6). Refer to Fig. 7.

EIS is both readable and writable.

• **Bit 5 ~ 0** Not used.

8. IOCF (Interrupt Mask Register)

7	6	5	4	3	2	1	0
-	-	-	-	-	EXIE	ICIE	TCIE

• **Bit 7 ~ 3** Not used.

• Individual interrupt is enabled by setting its associated control bit in the IOCF to "1".

• Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Fig. 9.

• **Bit 2 (EXIE)** EXIF interrupt enable bit.

0: disable EXIF interrupt

1: enable EXIF interrupt

• **Bit 1 (ICIE)** ICIF interrupt enable bit.

0: disable ICIF interrupt

1: enable ICIF interrupt

• **Bit 0 (TCIE)** TCIF interrupt enable bit.

0: disable TCIF interrupt

1: enable TCIF interrupt

• IOCF register is both readable and writable.

4.3 TCC/WDT & Prescaler

There is an 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available for the TCC only or the WDT only at the same time and the PAB bit of the CONT register is used to determine the prescaler assignment. The PSR0~PSR2 bits determine the ratio. The prescaler is cleared each time the instruction is written to TCC under TCC mode. The WDT and prescaler, when assigned to WDT mode, are cleared by the “WDTC” or “SLEP” instructions. Fig. 5 depicts the circuit diagram of TCC/WDT.

• R1(TCC) is an 8-bit timer/counter. The clock source of TCC can be internal or external clock input (edge selectable from TCC pin). If TCC signal source is from internal clock, TCC will increase by 1 at every instruction cycle (without prescaler). Referring to Fig. 5, CLK=Fosc/2 or CLK=Fosc/4, depends on the CODE Option bit CLK. CLK=Fosc/2 is used if CLK bit is "0", and CLK=Fosc/4 is used if CLK bit is "1". If TCC signal source is from external clock input, TCC is increased by 1 at every falling edge or rising edge of TCC pin.

• The watchdog timer is a free running on-chip RC oscillator. The WDT will keep running even when the oscillator driver has been turned off (i.e. in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during normal mode by software programming. Refer to WDTE bit of IOCE register. Without prescaler, the WDT time-out period is approximately 18 ms[1] (default).

4.4 I/O Ports

The I/O registers, both Port 5 and Port 6, are bi-directional tri-state I/O ports. Port 6 can be pulled-high

[1] <Note>: Vdd = 5V, set up time period = 16.5ms ± 30%

Vdd = 3V, set up time period = 18ms ± 30%

internally by software except P63. In addition, Port 6 can also have open-drain output by software except P63. Input status changed interrupt (or wake-up) function is available from Port 6. P50 ~ P52 and P60 ~ P62 pins can be pulled-down by software. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC6) except P63. The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5 and Port 6 are shown in Fig. 6,Fig.7 and fig. 8 respectively.

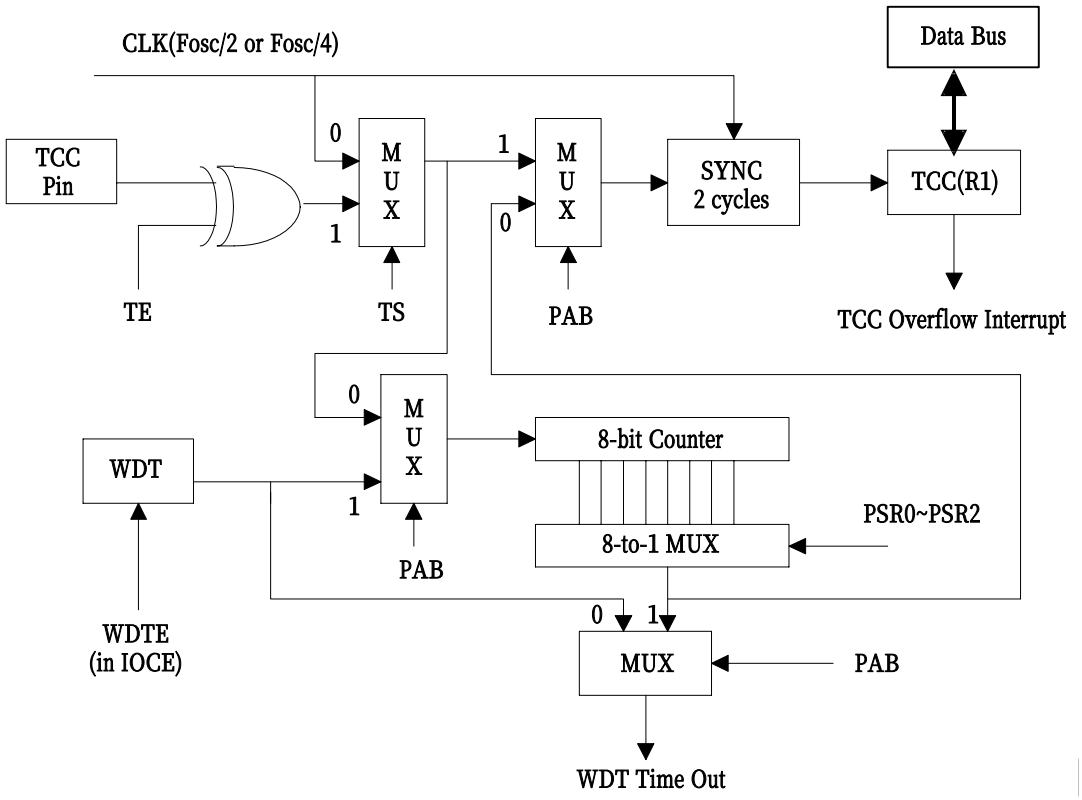
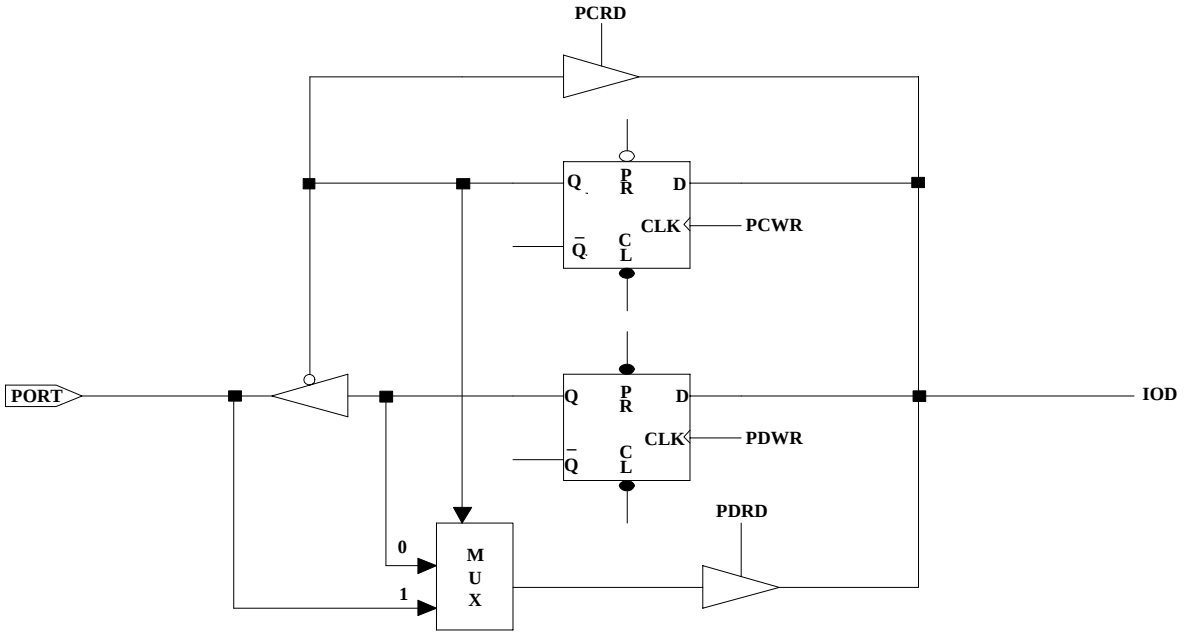
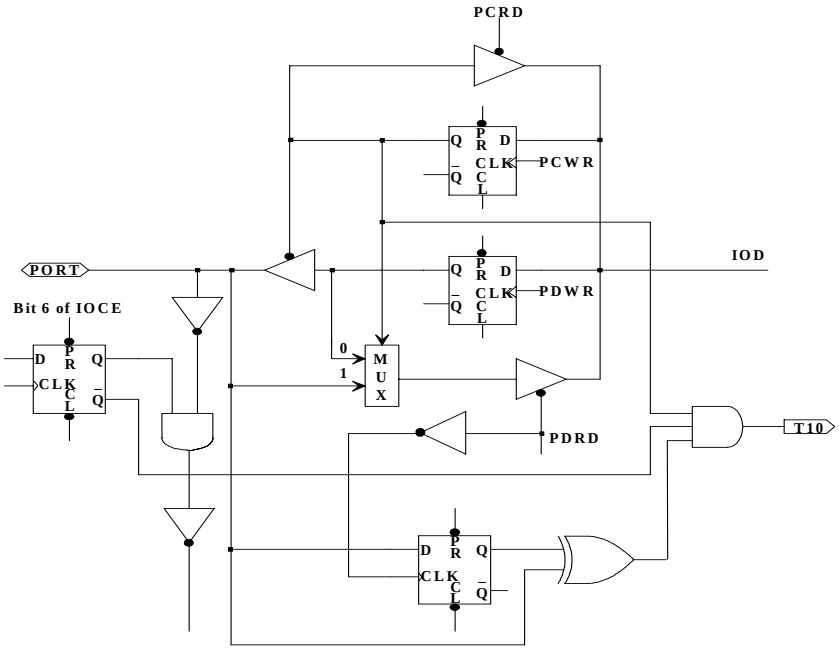


Fig. 5 Block diagram of TCC and WDT



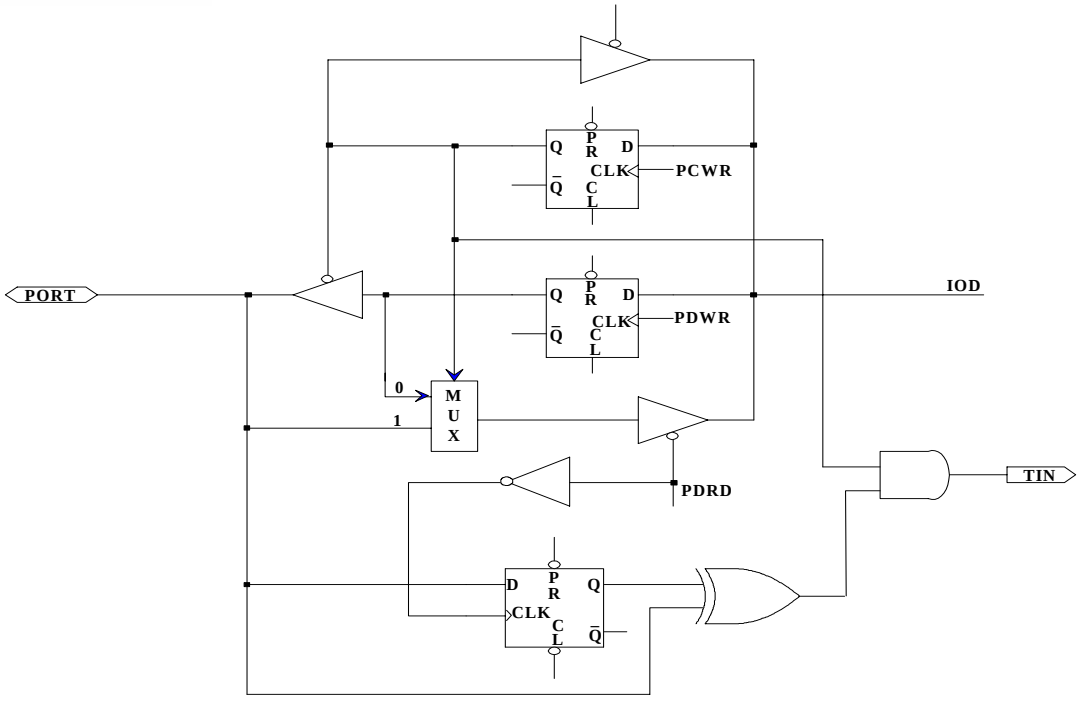
*Pull-down is not shown in the figure.

Fig. 6 The circuit of I/O port and I/O control register for Port 5



*Pull-high (down), Open-drain are not shown in the figure.

Fig. 7 The circuit of I/O port and I/O control register for P60(/INT)



*Pull-high (down), Open-drain are not shown in the figure.

Fig. 8 The circuit of I/O port and I/O control register for P61~P67

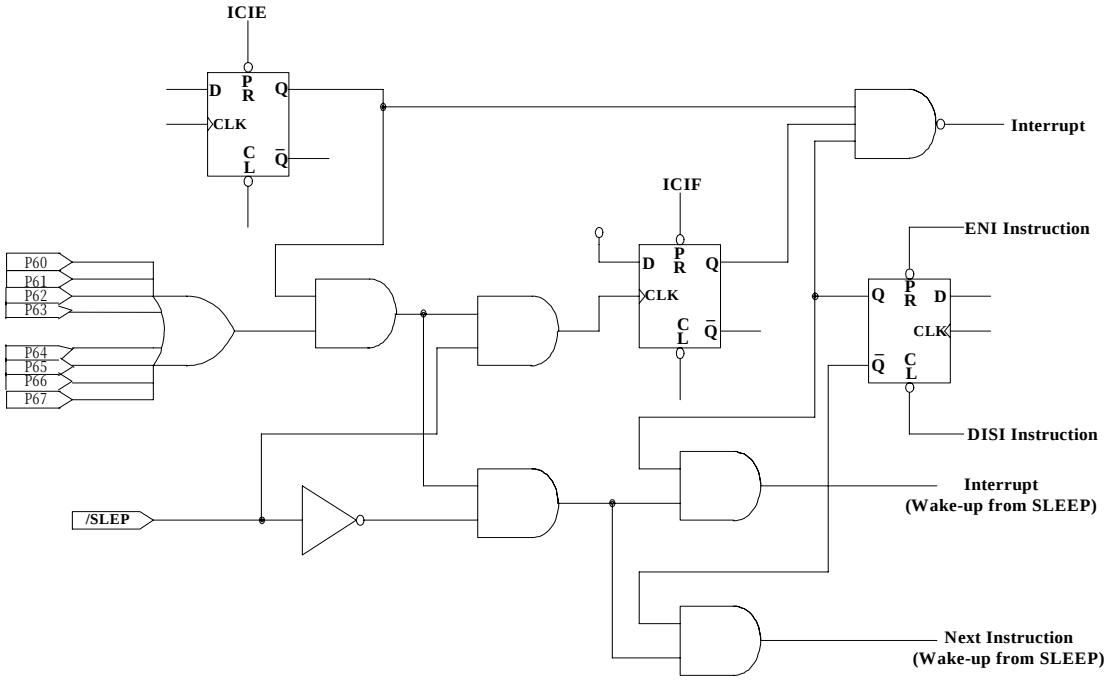


Fig. 9 Block diagram of I/O Port 6 with input change interrupt/wake-up

Table 2 Usage of Port 6 input change wake-up/interrupt function

Usage of Port 6 Input Status Change Wake-up/Interrupt	
(I) Wake-up from Port 6 Input Status Change (a) Before SLEEP 1. Disable WDT 2. Read I/O Port 6 (MOV R6,R6) 3. Execute "ENI" or "DISI" 4. Enable interrupt (Set IOCF.1) 5. Execute "SLEP" instruction (b) After Wake-up 1. IF "ENI" → Interrupt vector (008H) 2. IF "DISI" → Next instruction	**(II)** Port 6 Input Status Change Interrupt 1. Read I/O Port 6 (MOV R6,R6) 2. Execute "ENI" 3. Enable interrupt (Set IOCF.1) 4. IF Port 6 change (interrupt) → Interrupt vector (008H)

4.5 RESET and Wake-up

1. RESET

Input Status Change

(1) Power on reset.

(2) /RESET pin input "low", or

(3) WDT time-out (if enabled).

The device is kept in a RESET condition for a period of approx. 18ms[1] (one oscillator start-up timer period) after the reset is detected. Once the RESET occurs, the following functions are performed. Refer to Fig10..

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog timer and prescaler are cleared.
- When power is switched on, the upper 3 bits of R3 are cleared.
- The bits of the CONT register are set to all "1" except for the Bit 6 (INT flag).
- The bits of the IOCB register are set to all "1".
- The IOCC register is cleared.
- The bits of the IOCD register are set to all "1".
- Bit 7 of the IOCE register is set to "1", and Bits 4 and 6 are cleared.
- Bits 0~2 of RF and bits 0~2 of IOCF register are cleared.

[1] <Note> Vdd = 5V, set up time period = 16.5ms ± 30%

Vdd = 3V, set up time period = 18ms ± 30%

The sleep (power down) mode is attained by executing the “SLEP” instruction. While entering sleep mode, WDT (if enabled) is cleared but keeps on running. The controller can be awakened by

(1) External reset input on /RESET pin,

(2) WDT time-out (if enabled), or

(3) Port 6 input status changes (if enabled).

The first two cases will cause the EM78P153S to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). The last case is considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) decides whether or not the controller branches to the interrupt vector following wake-up. If ENI is executed before SLEP, the instruction will begin to execute from the address 008H after wake-up. If DISI is executed before SLEP, the operation will restart from the instruction right next to SLEP after wake-up.

Only one of the Cases 2 and 3 can be enabled before entering the sleep mode. That is,

[a] if Port 6 input status changed interrupt is enabled before SLEP , WDT must be disabled. by software. However, the WDT bit in the option register remains enabled. Hence, the EM78P153S can be awakened only by Case 1 or 3.

[b] if WDT is enabled before SLEP, Port 6 Input Status Change Interrupt must be disabled. Hence, the EM78P153S can be awakened only by Case 1 or 2. Refer to the section on interrupt.

If Port 6 Input Status Changed Interrupt is used to wake-up the EM78P153S (Case [a] above), the following instructions must be executed before SLEP:

```
MOV         A, @xxxx1110b   ; Select WDT prescaler, prescaler must set over 1:1
CONTW
WDTC                        ; Clear WDT and prescaler
MOV         A, @0xxxxxxxb   ; Disable WDT
IOW         RE
MOV         R6, R6          ; Read Port 6
MOV         A, @00000x1xb   ; Enable Port 6 input change interrupt
IOW         RF
ENI (or DISI)               ; Enable (or disable) global interrupt
SLEP                        ; Sleep
```

NOTE**:**

1. After waking up from the sleep mode, WDT is automatically enabled. The WDT enabled/disabled operation after waking up from sleep mode should be appropriately defined in the software

2. To avoid a reset from occurring when the Port 6 Input Status Changed Interrupt enters into interrupt vector or is used to wake-up the MCU, the WDT prescaler must be set above the 1:1 ratio.

Table 3 The Summary of the Initialized Register Values

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC5	Bit Name	X	X	X	X	C53	C52	C51	C50
		Power-On	0	0	0	0	1	1	1	1
		/RESET and WDT	0	0	0	0	1	1	1	1
		Wake-Up from Pin Change	0	0	0	0	P	P	P	P
N/A	IOC6	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x05	P5	Bit Name	X	X	X	X	P53	P52	P51	P50
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x06	P6	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	CONT	Bit Name	X	INT	TS	TE	PAB	PSR2	PSR1	PSR0
		Power-On	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-Up from Pin Change	P	0	P	P	P	P	P	P
0x00	R0(IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x01	R1(TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x02	R2(PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	N	P	P	P
0x03	R3(SR)	Bit Name	RST	GP1	GP0	T	P	Z	DC	C
		Power-On	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-Up from Pin Change	1	P	P	t	t	P	P	P
0x04	R4(RSR)	Bit Name	GP1	GP0	-	-	-	-	-	-
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0F	RF(ISR)	Bit Name	X	X	X	X	X	EXIF	ICIF	TCIF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	0	0	0	0	P	N	P
0x0B	IOCB	Bit Name	X	/PD6	/PD5	/PD4	/PD3	/PD2	/PD1	/PD0
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0C	IOCC	Bit Name	OD7	OD6	OD5	OD4	X	OD2	OD1	OD0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0D	IOCD	Bit Name	/PH7	/PH6	/PH5	/PH4	X	/PH2	/PH1	/PH0
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0E	IOCE	Bit Name	WDTE	EIS	X	X	X	X	X	X
		Power-On	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-Up from Pin Change	1	P	1	1	1	1	1	1
0x0F	IOCF	Bit Name	X	X	X	X	X	EXIE	ICIE	TCIE
		Power-On	1	1	1	1	1	0	0	0
		/RESET and WDT	1	1	1	1	1	0	0	0
		Wake-Up from Pin Change	1	1	1	1	1	P	P	P
0x10~0x2F	R10~R2F	Bit Name	-	-	-	-	-	-	-	-
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P

X: not used. U: unknown or don't care. -: not defined P: previous value before reset. t: check Table 4

N: Monitors interrupt operation status; 1 = running; P = not running

2. /RESET Configure

Refer to Fig. 10 When the RESET bit in the OPTION word is programmed to 0, the external /RESET is enabled. When programmed to 1, the internal /RESET is enabled, tied to the internal Vdd and the pin is defined as P63.

3. The status of RST, T, and P of STATUS register

A RESET condition is initiated by the following events:

1. A power-on condition,
2. A high-low-high pulse on /RESET pin, and
3. Watchdog timer time-out.

The values of RST, T and P, listed in Table 4 are used to check hoe the processor wakes up.

Table 5 shows the events which may affect the status of RST, T and P.

Table 4 The Values of RST, T and P after RESET

Reset Type	RST	T	P
Power on	0	1	1
/RESET during Operating mode	0	*P	*P
/RESET wake-up during SLEEP mode	0	1	0
WDT during Operating mode	0	0	P
WDT wake-up during SLEEP mode	0	0	0
Wake-Up on pin change during SLEEP mode	1	1	0

*P: Previous status before reset

Table 5 The Status of RST, T and P being Affected by Events

Event	RST	T	P
Power on	0	1	1
WDTC instruction	*P	1	1
WDT time-out	0	0	*P
SLEP instruction	*P	1	0
Wake-Up on pin change during SLEEP mode	1	1	0

*P: Previous value before reset

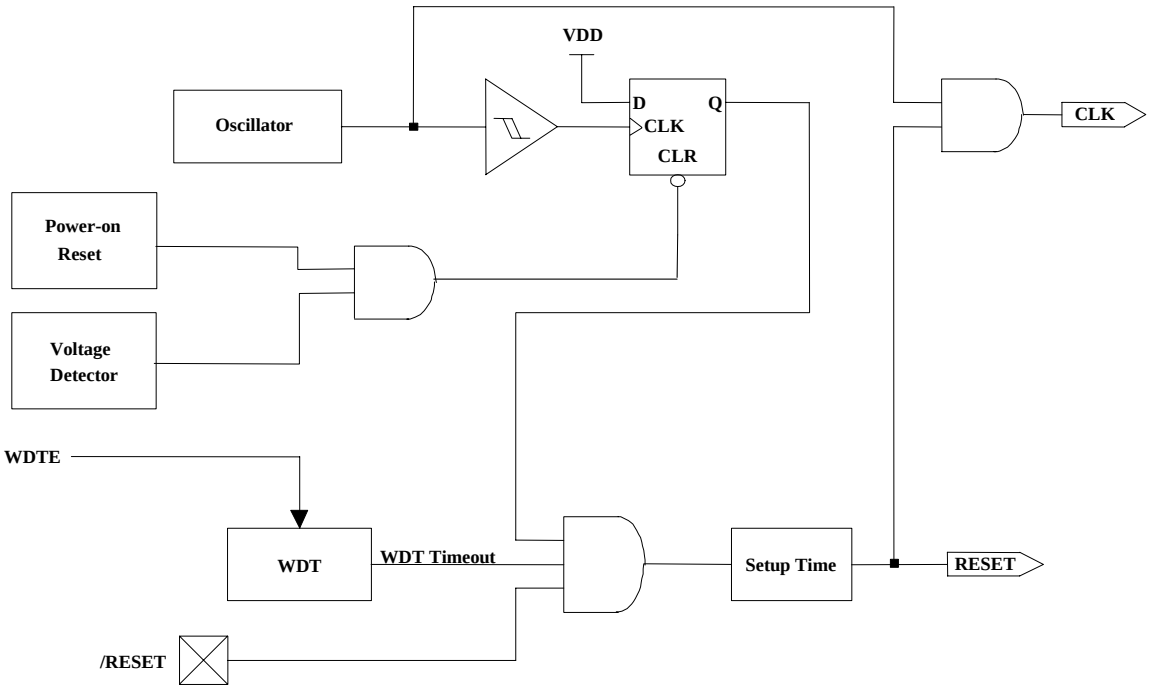


Fig. 10 Block Diagram of Controller Reset

4.6 Interrupt

The EM78P153S has three falling-edge interrupts as listed below:

(1) TCC overflow interrupt

(2) Port 6 Input Status Change Interrupt

(3) External interrupt [(P60, /INT) pin].

Before the Port 6 Input Status Changed Interrupt is enabled, reading Port 6 (e.g. "MOV R6,R6") is necessary. Each pin of Port 6 will have this feature if its status changes. Any pin configured as output or P60 pin configured as /INT, is excluded from this function. The Port 6 Input Status Changed Interrupt can wake up the EM78P153S from sleep mode if Port 6 is enabled prior to going into the sleep mode by executing SLEP instruction. When the chip wakes-up, the controller will continue to execute the program in-line if the global interrupt is disabled. If the global interrupt is enabled, it will branch to the interrupt vector 008H.

RF is the interrupt status register that records the interrupt requests in the relative flags/bits. IOCF is an interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (enabled) occurs, the next instruction will be fetched from address 008H. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in RF. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine before interrupts are enabled to avoid recursive interrupts.

The flag (except ICIF bit) in the Interrupt Status Register (RF) is set regardless of the status of its mask bit or the execution of ENI. Note that the outcome of RF will be the logic AND of RF and IOCF (refer to Fig. 11). The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

When an interrupt is generated by the INT instruction (enabled), the next instruction will be fetched from address 001H.

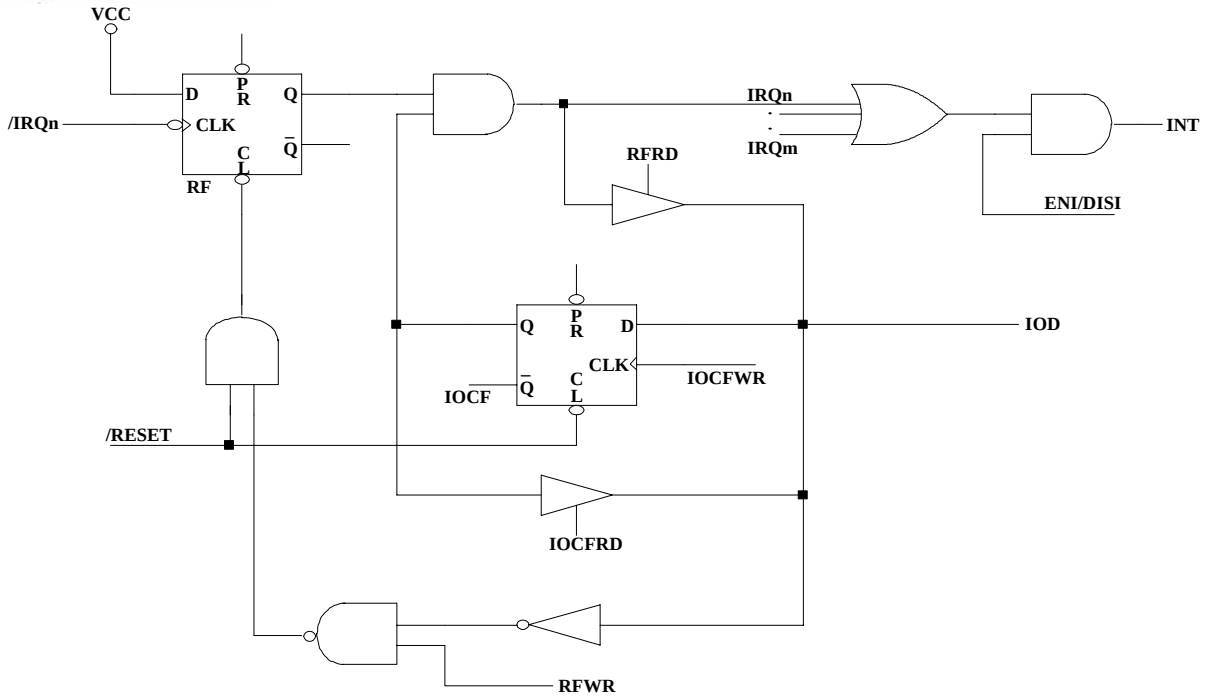


Fig. 11 Interrupt input circuit

4.7 Oscillator

1. Oscillator Modes

The EM78P153S can be operated in four different oscillator modes, such as Internal RC oscillator mode (IRC), External RC oscillator mode(ERC), High XTAL oscillator mode(HXT), and Low XTAL oscillator mode(LXT). User can select one of them by programming OCS1 and OSC2 in the CODE Option register. Table 6 depicts how these four modes are defined.

The up-limited operation frequency of crystal/resonator on the different VDDs is listed in Table 7.

Table 6 Oscillator Modes defined by OSC1 and OSC2

Mode	OSC1	OSC2
IRC(Internal RC oscillator mode)	1	1
ERC(External RC oscillator mode)	1	0
HXT(High XTAL oscillator mode)	0	1
LXT(Low XTAL oscillator mode)	0	0

<Note> The transient point of system frequency between HXT and LXY is around 400 KHz.

Table 7 The summary of maximum operating speeds

Conditions	VDD	Fxt max.(MHz)
Two cycles with two clocks	2.3	4.0
	3.0	8.0
	5.0	20.0

2. Crystal Oscillator/Ceramic Resonators(XTAL)

EM78P153S can be driven by an external clock signal through the OSCI pin as shown in Fig. 12.

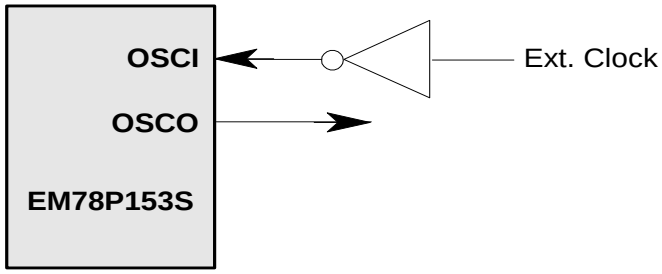


Fig. 12 Circuit for External Clock Input

In most applications, pin OSCI and pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Fig. 13 depicts such circuit. The same thing applies whether it is in the HXT mode or in the LXT mode. Table 8 provides the recommended values of C1 and C2. Since each resonator has its own attribute, user should refer to its specification for appropriate values of C1 and C2. RS, a serial resistor, may be necessary for AT strip cut crystal or low frequency mode

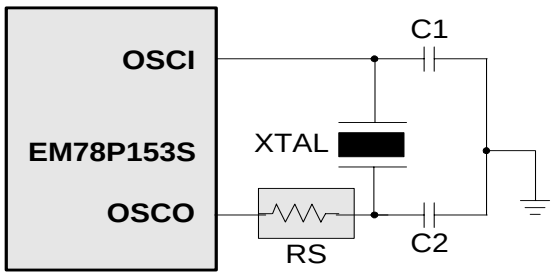


Fig. 13 Circuit for Crystal/Resonator

Table 8 Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonators

Oscillator Type	Frequency Mode	Frequency	C1(pF)	C2(pF)
Ceramic Resonators	HXT	455 kHz	100~150	100~150
		2.0 MHz	20~40	20~40
		4.0 MHz	10~30	10~30
Crystal Oscillator	LXT	32.768kHz	25	15
		100KHz	25	25
		200KHz	25	25
	HXT	455KHz	20~40	20~150
		1.0MHz	15~30	15~30
		2.0MHz	15	15
		4.0MHz	15	15

<Note> 1. The value of capacitors (C1, C2) is for reference.

3. External RC Oscillator Mode

For some applications that do not need to have its timing to be calculated precisely, the RC oscillator (Fig. 16) offers a lot of cost savings. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to the manufacturing process variation.

In order to maintain a stable system frequency, the values of the Cext should not be less than 20pF, and that the value of Rext should not be greater than 1 M ohm. If they cannot be kept in this range, the frequency is easily affected by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 KΩ, the oscillator becomes unstable because the NMOS cannot discharge the current of the capacitance correctly.

Based on the reasons above, it must be kept in mind that all of the supply voltage, the operation temperature, the components of the RC oscillator, the package types, the way the PCB is layout, will affect the system frequency.

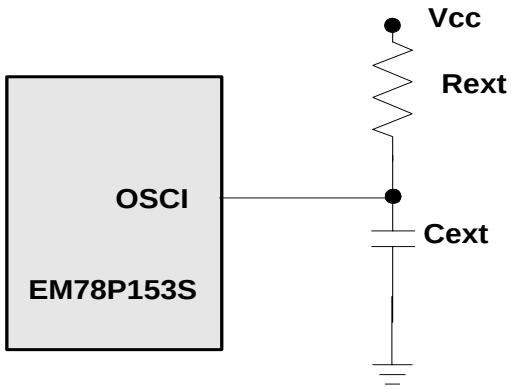


Fig.14 Circuit for External RC Oscillator Mode

Table 9 RC Oscillator Frequencies

Cext	Rext	Average Fosc 5V,25°C	Average Fosc 3V,25°C
20 pF	3.3k	3.92 MHz	3.63MHz
	5.1k	2.67 MHz	2.6 MHz
	10k	1.4 MHz	1.4 MHz
	100k	150 KHz	156 KHz
100 pF	3.3k	1.4 MHz	1.33 MHz
	5.1k	940 KHz	917 KHz
	10k	476 KHz	480 KHz
	100k	50 KHz	52 KHz
300 pF	3.3k	595 KHz	570 KHz
	5.1k	400 KHz	384 KHz
	10k	200 KHz	203 KHz
	100k	20.9 KHz	20 KHz

<Note> 1. Measured on DIP packages.

2. Design reference only

3. The frequency drift is about ±30%

4. Internal RC Oscillator Mode

EM78P153S offer a versatile internal RC mode with default frequency value of 4MHz.Internal RC oscillator mode still has other frequencies 8MHz, 1MHz, and 455KHz and can be set by OPTION bits, RCM1 and RCM0. All these four main frequencies can be calibration by programming the OPTION bits, CAL0~CAL2. Table 10 describes the EM78P153S internal RC drift with the variation of voltage, temperature, and process.

Table 10 Internal RC Drift Rate (Ta=25°C , VDD=5 V± 5%, VSS=0V)

Internal RC	Drift Rate			
	Temperature (0°C~70°C)	Voltage (2.3V~5.5V)	Process	Total
8MHz	± 3%	± 5%	± 10%	± 18%
4MHz	± 3%	± 5%	± 5%	± 13%
1MHz	± 3%	± 5%	± 10%	± 18%
455kHz	± 3%	± 5%	± 10%	± 18%

4.8 Code Option Register

The EM78P153S has one CODE option word that is not a part of the normal program memory. The option bits cannot be accessed during normal program execution.

Code Option Register and Customer ID Register arrangement distribution:

Word 0	Word1	Word 2
Bit12~Bit0	Bit1~Bit0	Bit12~Bit0

Code Option Register (Word 0)

WORD 0												
Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
/RESET	/ENWDT	CLKS	OSC1	OCS0	CS	SUT1	SUT0	TYPE	RCOUT	C2	C1	C0

• **Bit 12 (/RESET**): Define pin7 as a reset pin.

0: /RESET enable

1: /RESET disable

• **Bit 11 (/ENWTD**): Watchdog timer enable bit.

0: Enable

1: Disable

<Note> This bit must enable and the WDTE reg. (IOCE reg. bit 6) must disable when port 6 pin change wake up function is used.

• **Bit 10 (CLKS)**: Instruction period option bit.

0: two oscillator periods.

1: four oscillator periods.

Refer to the section of Instruction Set.

• **Bit 9 and Bit 8 (OSC1 and OSC0)**: Oscillator Modes Selection bits.

Table 11 Oscillator Modes defined by OSC1 and OSC0

Mode	OSC1	OSC0
IRC(Internal RC oscillator mode)	1	1
ERC(External RC oscillator mode)	1	0
HXT(High XTAL oscillator mode)	0	1

LXT(Low XTAL oscillator mode)	0	0

<Note> : The transient point of system frequency between HXT and LXY is around 400 KHz.

• **Bit 7 (CS)**: Code Security Bit

0: Security On

1: Security Off

• **Bit6 and Bit5 (SUT1 and SUT0)**: Set-Up Time of device bits.

Table 12 Set-Up Time of device Programming

SUT1	SUT0	*Set-Up Time
1	1	18 ms
1	0	4.5 ms
0	1	288 ms
0	0	72 ms

* Theoretical values, for reference only

• **Bit 4 (Type)**: Type selection for EM78P153S

TYPE	Series
0	EM78P153S
1	X

• **Bit 3 (RCOUT)**: A selecting bit of Oscillator output or I/O port.

RCOUT	Pin Function
0	P64
1	OSCO

• **Bit 2, Bit 1, and Bit 0 (C2, C1, C 0)**: Calibrator of internal RC mode Bit 3

C2,C1,C0 must be set to “1” ONLY.

Code Option Register (Word 1)

WORD1	
Bit1	Bit0
RCM1	RCM0

Bit 1, and Bit 0 (RCM1, RCM0): RC mode selection bits

RCM 1	RCM 0	*Frequency(MHz)
1	1	4
1	0	8
0	1	1
0	0	455kHz

Customer ID Register (Word 2)

Bit 12~Bit 0
XXXXXXXXXXXX

Bit 12~ 0 : Customer’s ID code

4.9 Power On Considerations

Any microcontroller is not guaranteed to start to operate properly before the power supply stabilizes at its steady state. Under customer application, when power is OFF, Vdd must drop to below 1.8V and remains OFF for 10us before power can be switched ON again. This way, the EM78P153S will reset and work normally. The extra external reset circuit will work well if Vdd can rise at very fast speed (50 ms or less). However, under most cases where critical applications are involved, extra devices are required to assist in solving the power-up problems.

4.10 Programmable Oscillator Set-Up Time

The Option word contains SUT0 and SUT1 which can be used to define the oscillator set up time. Theorically, the range is from 4.5 ms to 72 ms. For most of crystal or ceramic resonators, the lower the operation frequency is, the longer the Set-up time may be required. Table 12 describes the values of Oscillator Set-Up Time.

4.11 External Power On Reset Circuit

The circuit shown in Fig 17 implements an external RC to produce the reset pulse. The pulse width (time constant) should be kept long enough for Vdd to reach minimum operation voltage. This circuit is used when the power supply has slow rise time. Because the current leakage from the /RESET pin is about ±5μA, it is recommended that R should not be great than 40 K. In this way, the voltage in pin /RESET will be held below 0.2V. The diode (D) acts as a short circuit at the moment of power down. The capacitor C, will discharged rapidly and fully. Rl, the current-limited resistor, will prevent high current discharge or ESD (electrostatic discharge) from flowing to pin /RESET.

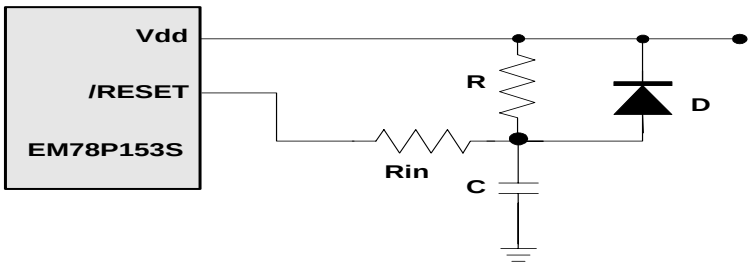


Fig. 15 External Power-Up Reset Circuit

4.12 Residue-Voltage Protection

When battery is replaced, device power (Vdd) is taken off but residue-voltage remains. The

residue-voltage may trips below Vdd minimum, but not to zero. This condition may cause a poor power on reset. Fig.18 and Fig. 19 show how to build a residue-voltage protection circuit.

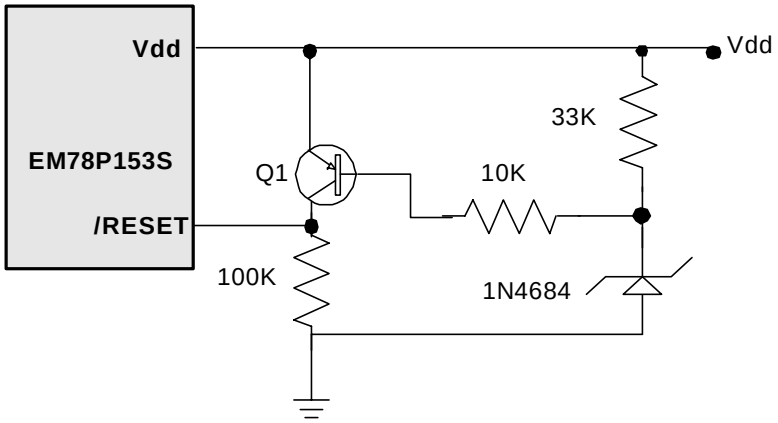


Fig. 16 Circuit 1 for the residue voltage protection

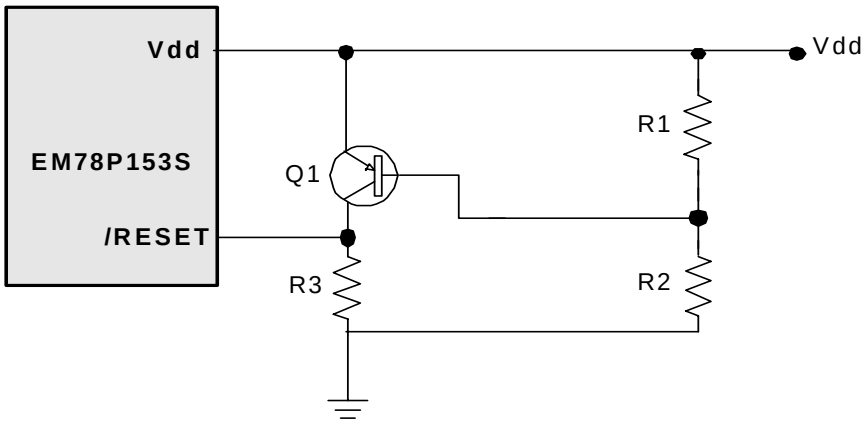


Fig.17 Circuit 2 for the residue voltage protection

4.13 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2,A",

"ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g. "SUB R2,A", "BS(C) R2,6", "CLR R2", ····). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows:

(A) Modify one instruction cycle to consist of 4 oscillator periods.

(B) Execute within two instruction cycles the "JMP", "CALL", "RET", "RETL", "RETI" commands, or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") which were tested to be true. The instructions that are written to the program counter, should also take two instruction cycles.

The Case (A) is selected by the CODE Option bit, called CLKS. One instruction cycle will consist of two oscillator clocks if CLKS is low, and four oscillator clocks if CLKS is high.

Note that once the 4 oscillator periods within one instruction cycle is selected under Case (A), the internal clock source to TCC should be CLK=Fosc/4 ,instead of Fosc/ 2 as illustrated in Fig. 5.

In addition, the instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

The symbol "R" represents a register designator that specifies which one of the registers (including operational registers and general purpose registers) is to be utilized by the instruction. "b" represents a bit field designator that selects the value for the bit which is located in the register "R", and affects the operation. "k" represents an 8 or 10-bit constant or literal value.

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P
0 0000 0000 0100	0004	WDTC	0 → WDT	T,P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None <Note1>
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None <Note1>
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z

0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z,C,DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z,C,DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ VR → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ VR → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z,C,DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z,C,DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1),R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1),R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1),R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1),R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7),R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None <Note2>
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None <Note3>
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP],(Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A,[Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z,C,DC
1 1110 0000 0001	1E01	INT	PC+1 → [SP],001H → PC	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z,C,DC

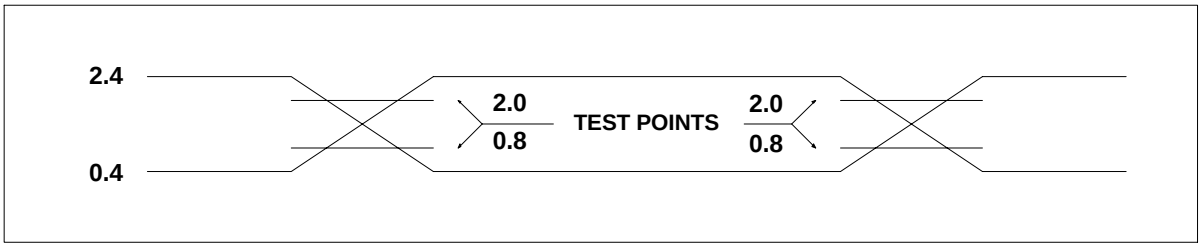
<Note 1> This instruction is applicable to IOC5~IOC6, IOCB~IOCF only.

<Note 2> This instruction is not recommended for RF operation.

<Note 3> This instruction cannot operate under RF.

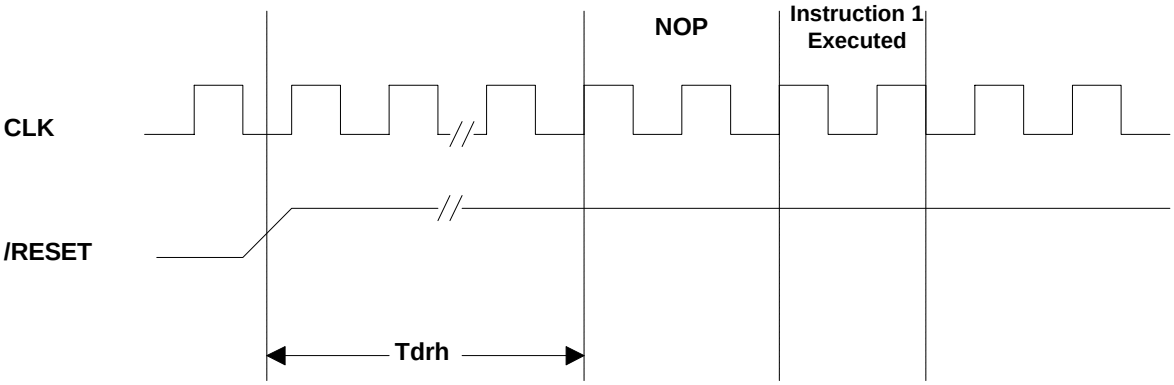
4.14 Timing Diagrams

AC Test Input/Output Waveform

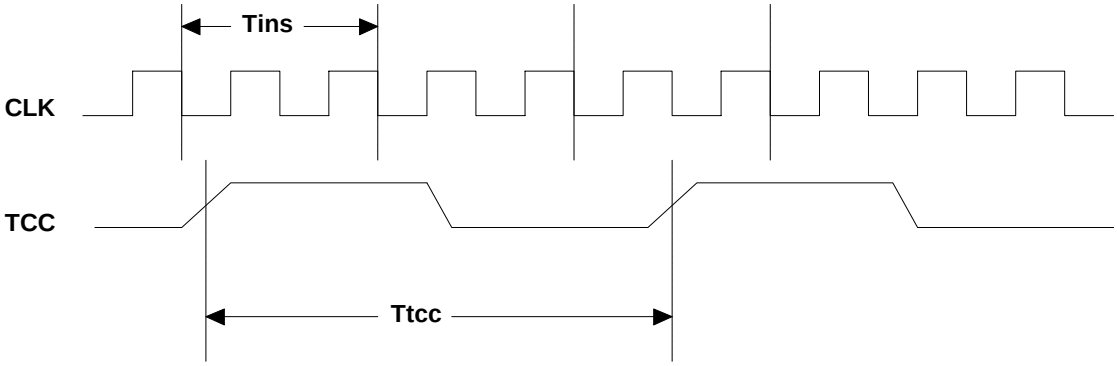


AC Testing : Input is driven at 2.4V for logic "1",and 0.4V for logic "0".Timing measurements are made at 2.0V for logic "1",and 0.8V for logic "0".

RESET Timing (CLK="0")



TCC Input Timing (CLKS="0")



5. ABSOLUTE MAXIMUNM RATINGS

Items	Rating
Temperature under bias	0°C to 70°C
Storage temperature	-65°C to 150°C
Input voltage	-0.3V to +6.0V
Output voltage	-0.3V to +6.0V

6. ELECTRICAL CHARACTERISTIC

6.1 DC Electrical Characteristic

(Ta= 0°C ~ 70 °C, VDD= 5.0V±5%, VSS= 0V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Fxt	XTAL: VDD to 2.3V	Two cycle with two clocks	DC		4.0	MHz
Fxt	XTAL: VDD to 3V	Two cycle with two clocks	DC		8.0	MHz
Fxt	XTAL: VDD to 5V	Two cycle with two clocks	DC		20.0	MHz
ERC	RC: VDD to 5V	R: 5KΩ, C: 39 pF	F-30%	1500	F+30%	KHz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS			±1	μA
VIH1	Input High Voltage (VDD=5.0V)	Ports 5, 6	2.0			V
VIL1	Input Low Voltage (VDD=5.0V)	Ports 5, 6			0.8	V
VIHT1	Input High Threshold Voltage (VDD=5.0V)	/RESET, TCC (Schmitt trigger)	2.0			V
VILT1	Input Low Threshold Voltage (VDD=5.0V)	/RESET, TCC (Schmitt trigger)			0.8	V
VIHX1	Clock Input High Voltage (VDD=5.0V)	OSCI	2.5			V
VILX1	Clock Input Low Voltage (VDD=5.0V)	OSCI			1.0	V
VIH2	Input High Voltage (VDD=3.0V)	Ports 5, 6	1.5			V
VIL2	Input Low Voltage (VDD=3.0V)	Ports 5, 6			0.4	V
VIHT2	Input High Threshold Voltage (VDD=3.0V)	/RESET, TCC (Schmitt trigger)	1.5			V
VILT2	Input Low Threshold Voltage (VDD=3.0V)	/RESET, TCC (Schmitt trigger)			0.4	V
VIHX2	Clock Input High Voltage (VDD=3.0V)	OSCI	1.5			V
VILX2	Clock Input Low Voltage (VDD=3.0V)	OSCI			0.6	V
VOH1	Output High Voltage (Ports 5, 6) (P60~P63, P66~P67 are Schmitt trigger)	IOH = -12.0 mA	2.4			V
VOL1	Output Low Voltage (P50~P53, P60~P63, P66~P67), (P60~P63, P66~P67 are Schmitt trigger)	IOL = 12.0 mA			0.4	V
VOL2	Output Low Voltage (P64,P65)	IOL = 16.0 mA			0.4	V
IPH	Pull-high current	Pull-high active, input pin at VSS	-50	-100	-240	μA
IPD	Pull-down current	Pull-down active, input pin at VDD	20	50	120	μA
ISB1	Power down current	All input and I/O pins at VDD, output pin floating, WDT disabled			1	μA
ISB2	Power down current	All input and I/O pins at VDD, output pin floating, WDT enabled			10	μA
ICC1	Operating supply current(VDD=3V) at two clocks	/RESET= 'High', Fosc=32KHz (Crystal type,CLKS="0"), output pin floating, WDT disabled	15	15	30	μA
ICC2	Operating supply current (VDD=3V) at two clocks	/RESET= 'High', Fosc=32KHz (Crystal type,CLKS="0"), output pin floating, WDT enabled		19	35	μA
ICC3	Operating supply current(VDD=5.0V) At two clocks	/RESET= 'High', Fosc=4MHz (Crystal type, CLKS="0"), output pin floating			2.0	mA
ICC4	Operating supply current(VDD=5.0V) at two clocks	/RESET= 'High', Fosc=10MHz (Crystal type, CLKS="0"), output pin floating			4.0	mA

* These parameters are characterizes and tested.

* Data in the Minimum, Typical, Maximum("Min","Typ","Max") column are based on characterization results at 25℃. This data is for design guidance and is tested.

6.2 AC Electrical Characteristic

(Ta=0°C ~ 70 °C, VDD=5V±5%, VSS=0V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle		45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	100		DC	ns
		RC type	500		DC	ns
Ttcc	TCC input period		(Tins+20)/N*			ns
Tdrh	Device reset hold time	Ta = 25°C TXAL,SUT1,SUT0=1,1	17.6-30%	17.6	17.6+30%	ms
Trst	/RESET pulse width	Ta = 25°C	2000			ns
Twdt1*	Watchdog timer period	Ta = 25°C SUT1,SUT0=1,1	17.6-30%	17.6	17.6+30%	ms
Twdt2*	Watchdog timer period	Ta = 25°C SUT1,SUT0=1,0	4.5-30%	4.5	4.5+30%	ms
Twdt3*	Watchdog timer period	Ta = 25°C SUT1,SUT0=0,1	288-30%	288	288+30%	ms
Twdt4*	Watchdog timer period	Ta = 25°C SUT1,SUT0=0,0	72-30%	72	72+30%	ms
Tset	Input pin setup time			0		ns
Thold	Input pin hold time			20		ns
Tdelay	Output pin delay time	Cload=20pF		50		ns

* Twdt1: The Option word (SUT1,SUT0) is used to define the oscillator Set-Up time. In Crystal mode the WDT timeout length is the same as set-up time(18ms).
* Twdt2: The Option word (SUT1,SUT0) is used to define the oscillator Set-Up time. In Crystal mode the WDT timeout length is the same as set-up time(4.5ms).
* Twdt3: The Option word (SUT1,SUT0) is used to define the oscillator Set-Up time. In Crystal mode the WDT timeout length is the same as set-up time(288ms).
* Twdt4: The Option word (SUT1,SUT0) is used to define the oscillator Set-Up time. In Crystal mode the WDT timeout length is the same as set-up time(72ms).
* These parameters are characterizes but not tested.
* Data in the Minimum, Typical, Maximum("Min","Typ","Max") column are based on characterization results at 25℃. This data is for design guidance and is not tested.
* N= selected prescaler ratio.
* The duration of watch dog timer is determined by option code (bit6,bit5)

6.3 Device Characteristic

The graphs provided in the following pages were derived based on a limited number of samples and are shown here for reference only. The device characteristic illustrated herein are not guaranteed for it accuracy. In some graphs, the data maybe out of the specified warranted operating range.

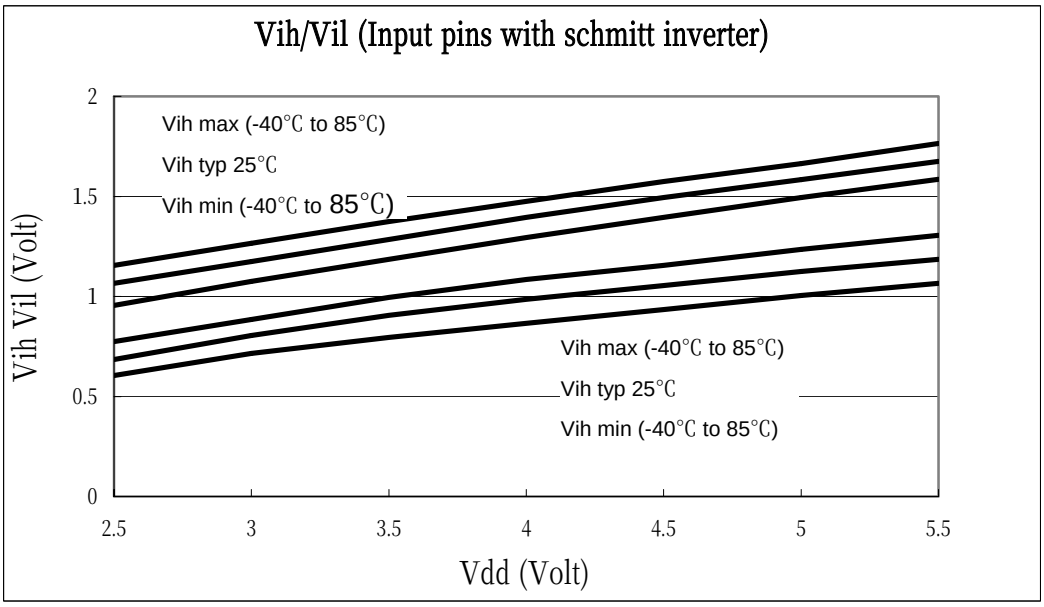


Fig. 18 Vih, Vil of P60~P63, P66, P67 vs. VDD

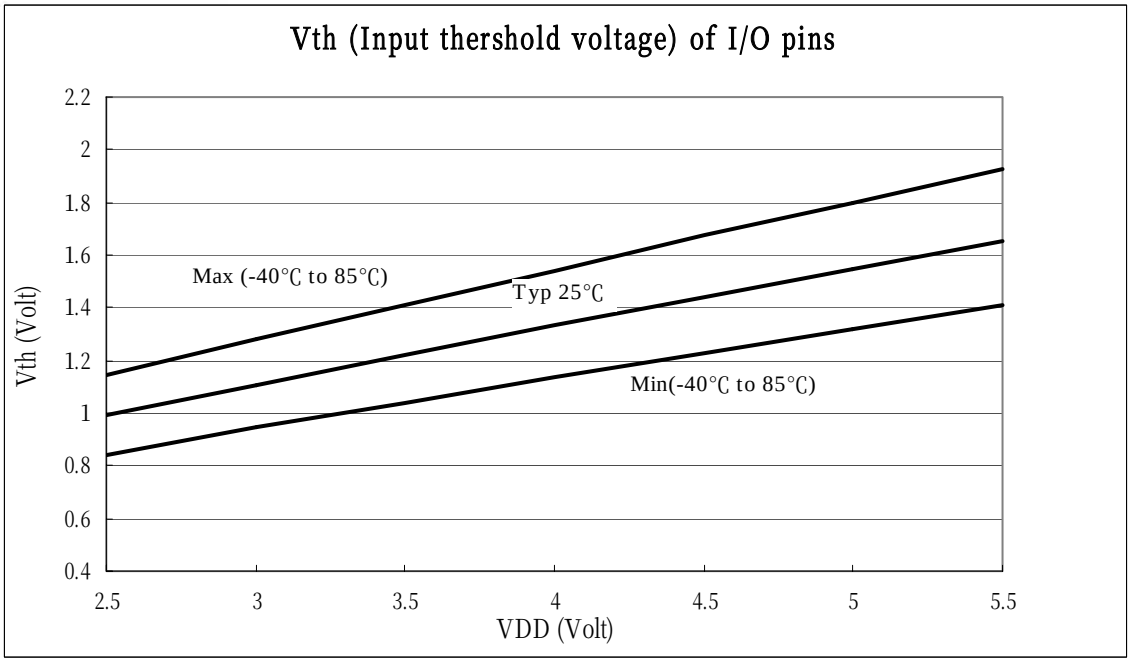


Fig. 19 Vth (Threshold voltage) of P50~P53, P64~P65 vs. VDD

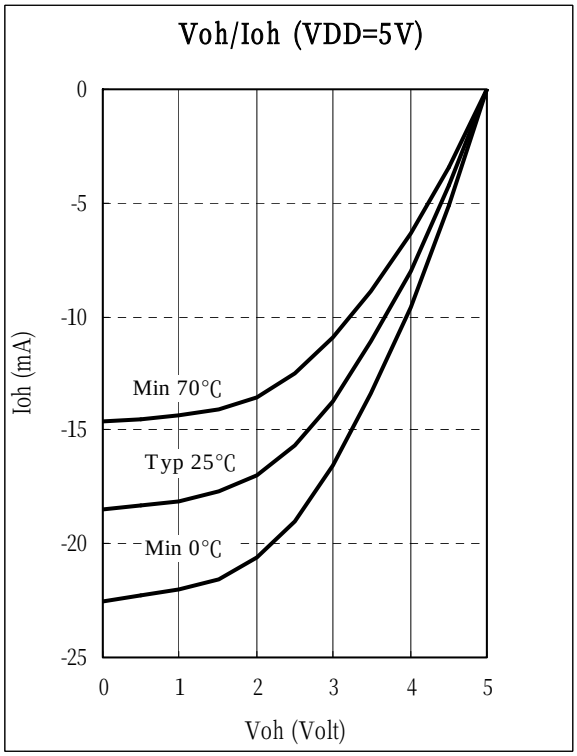


Fig. 20 Port5 and Port6 Voh vs. Ioh, VDD=5V

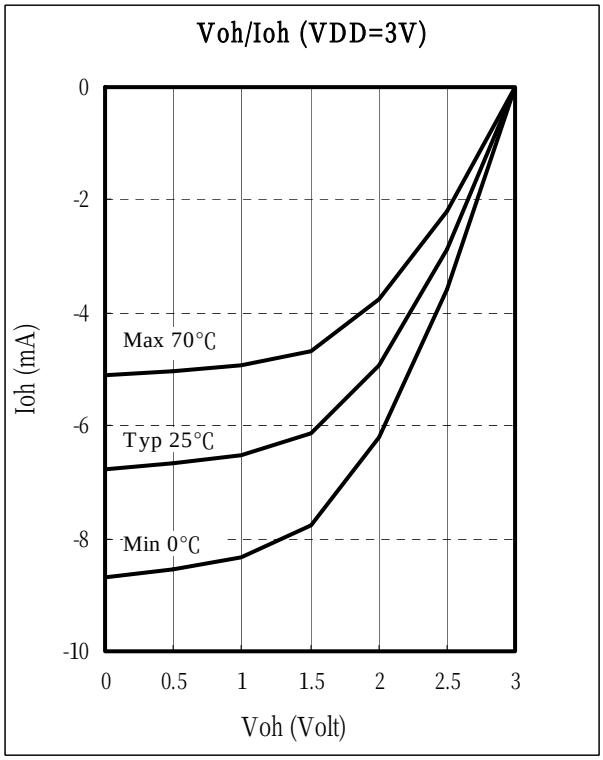


Fig. 21 Port5 and Port6 Voh vs. Ioh, VDD=3V

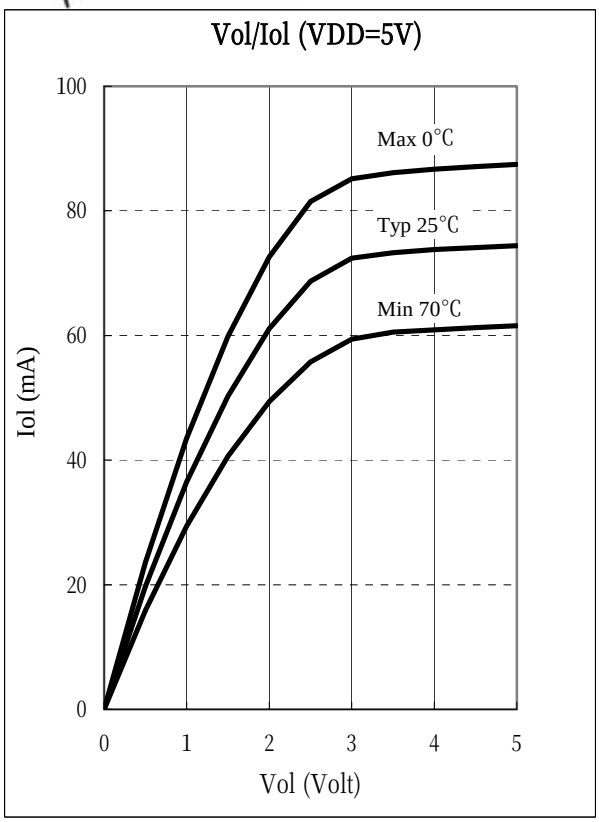


Fig. 22 Port5, Port6.0~Port6.3 and Port6.6~Port6.7 Vol vs. Iol, VDD=5V

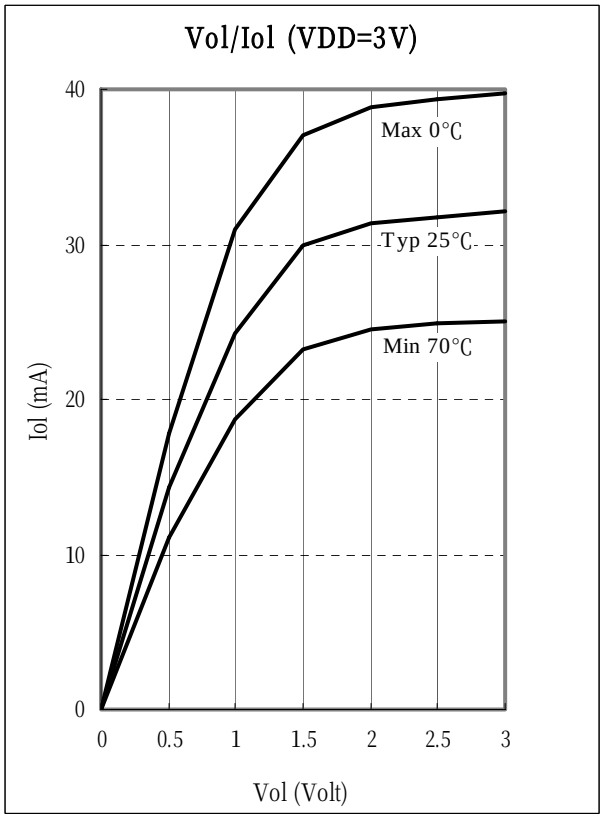


Fig. 23 Port5, Port6.0~Port6.3 and Port6.6~Port6.7 Vol vs. Iol, VDD=3V

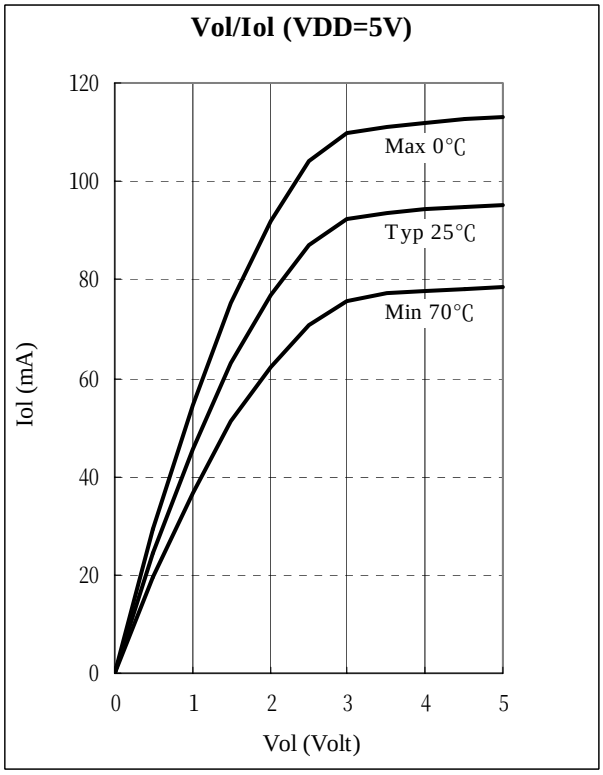


Fig. 24 Port6.4 and Port6.5 Vol vs. Iol, VDD=5V

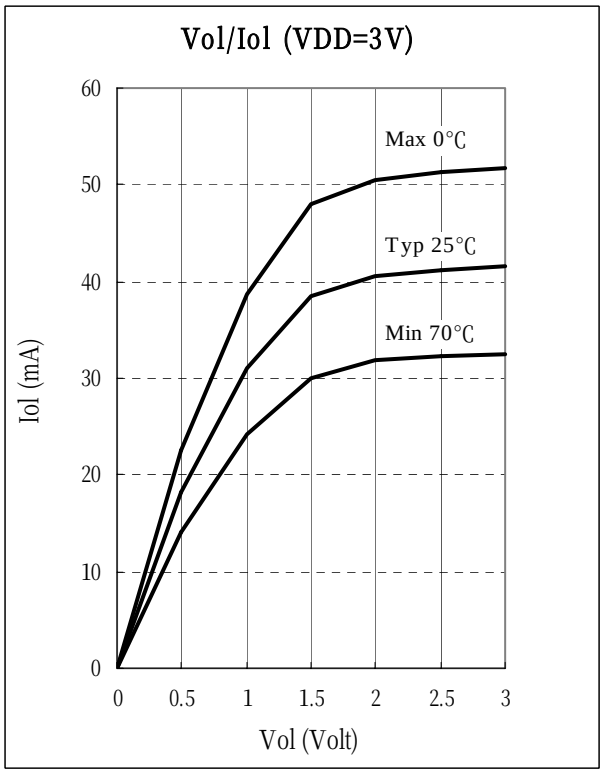


Fig. 25 Port6.4 and Port6.5 Vol vs. Iol, VDD=3V

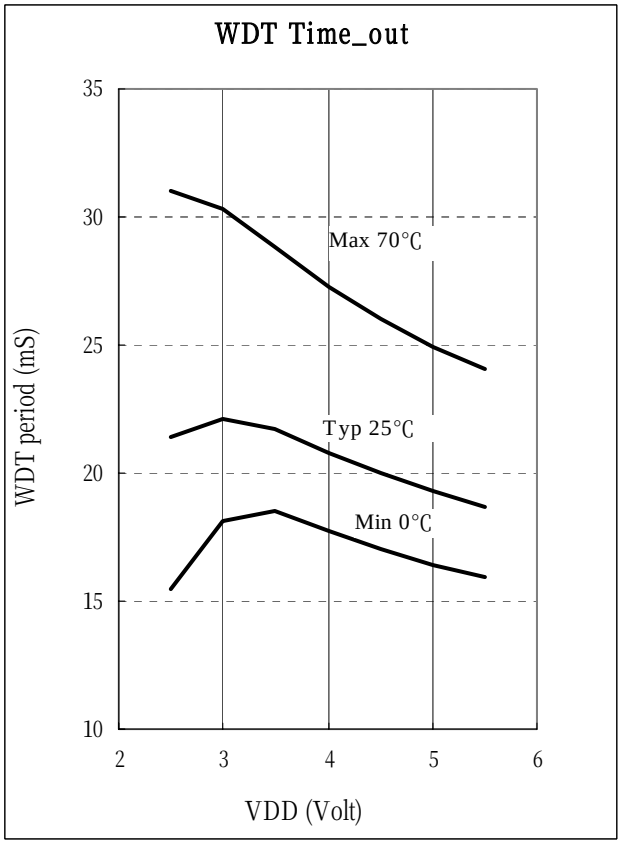


Fig. 26 WDT time out period vs. VDD, perscaler set to 1:1

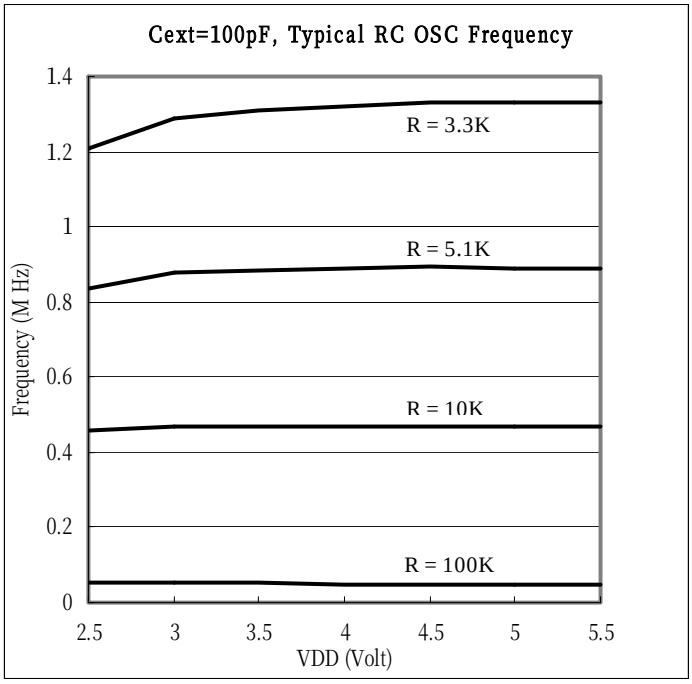


Fig. 27 Typical RC OSC Frequency vs. VDD

(Cext=100pF, Temperature at 25°C)

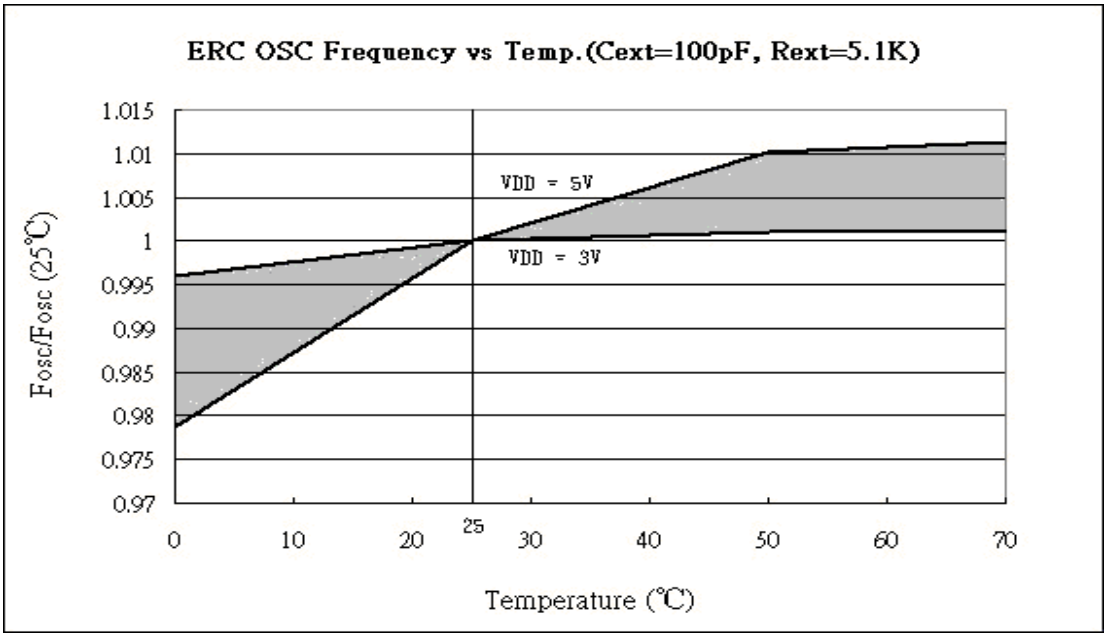


Fig. 28 Typical RC OSC Frequency vs. Temperature (R and C are ideal components)

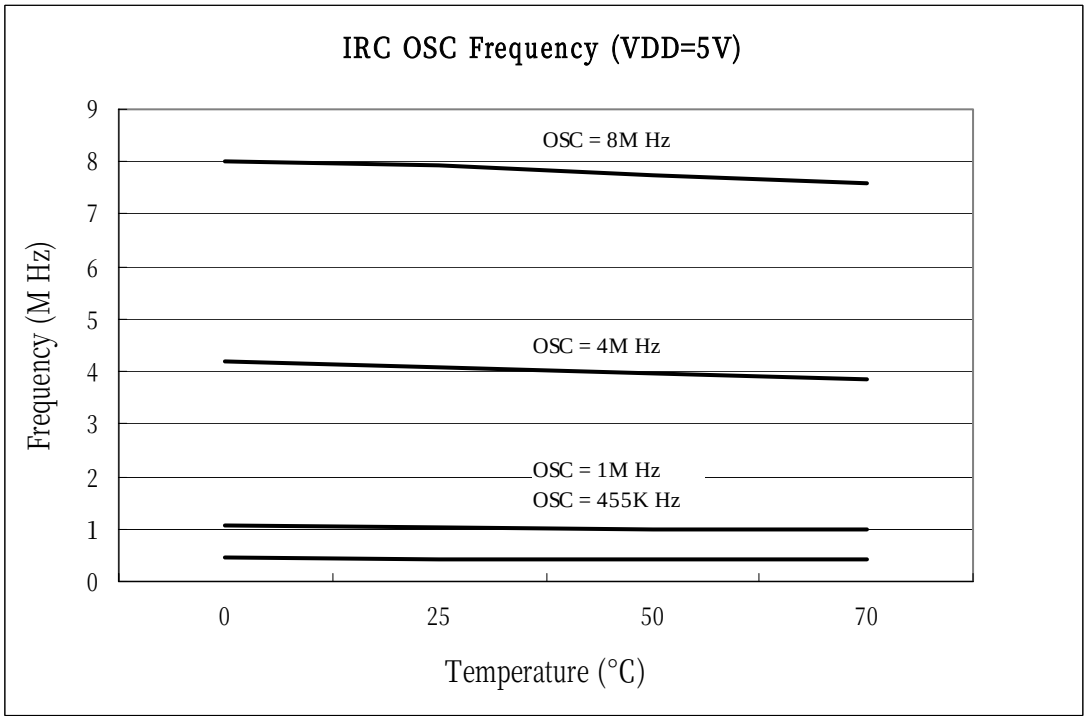


Fig. 29 Internal RC OSC Frequency vs. Temperature, VDD=5V

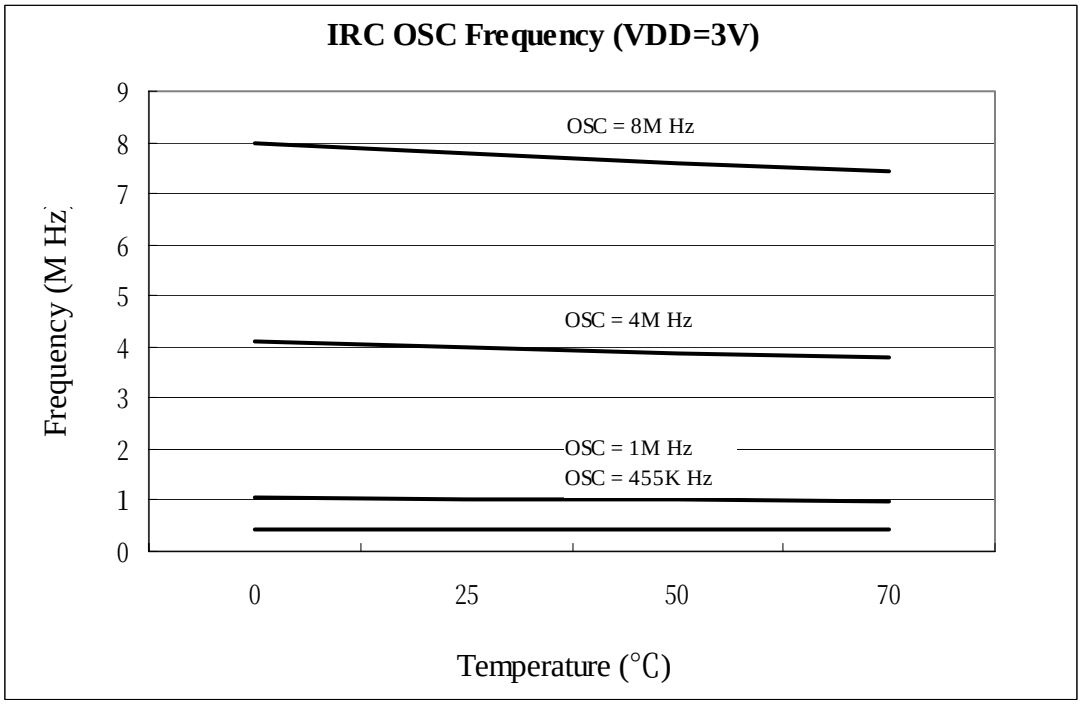


Fig. 30 Internal RC OSC Frequency vs. Temperature, VDD=3V

Four conditions exist with the Operating Current ICC1 to ICC4. These conditions are as follows:

ICC1: VDD=3V, Fosc=32K Hz, 2 clocks, WDT disable

ICC2: VDD=3V, Fosc=32K Hz, 2 clocks, WDT enable

ICC3: VDD=5V, Fosc=4M Hz, 2 clocks, WDT enable

ICC4: VDD=5V, Fosc=10M Hz, 2 clocks, WDT enable

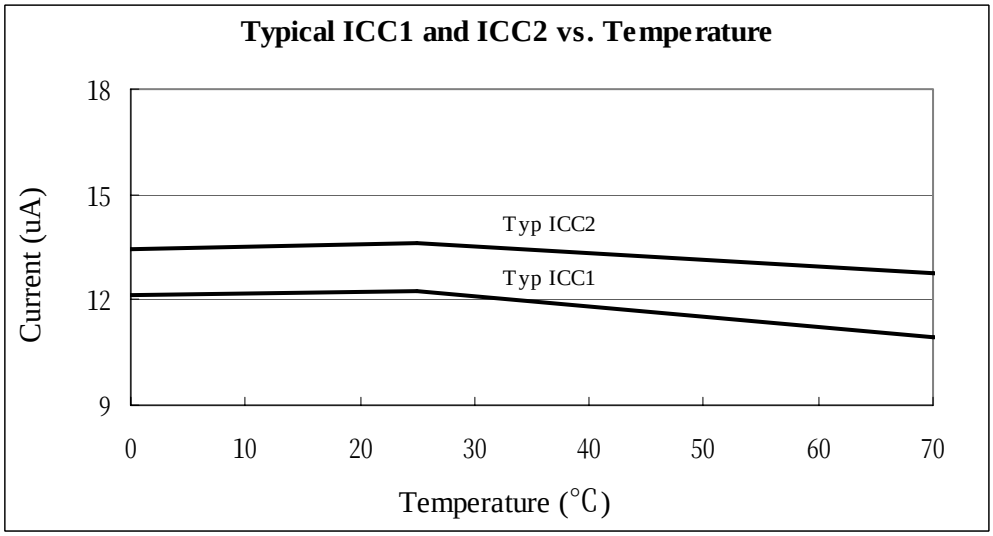


Fig. 31 Typical operating current (ICC1 and ICC2) vs. Temperature

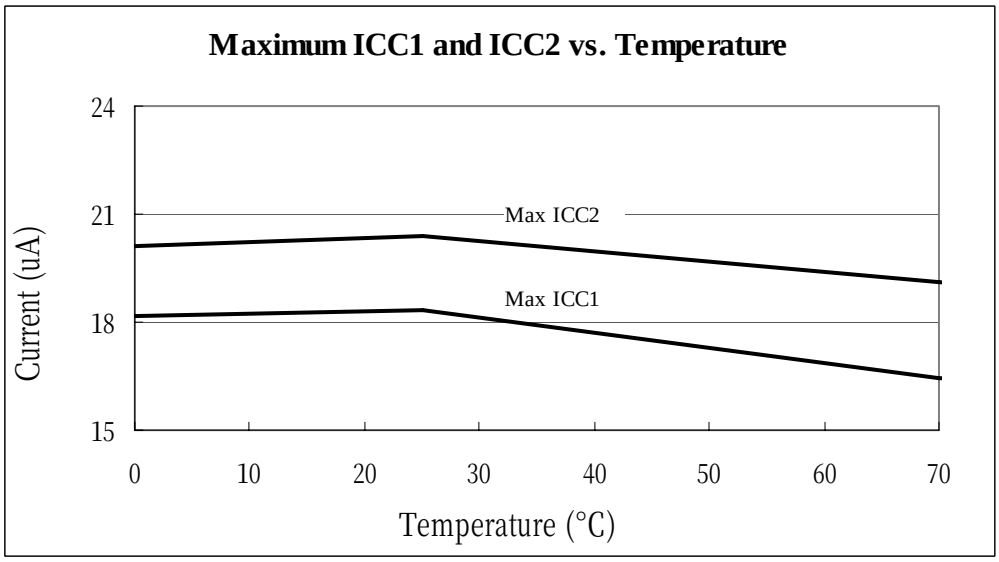


Fig. 32 Maximum operating current (ICC1 and ICC2) vs. Temperature

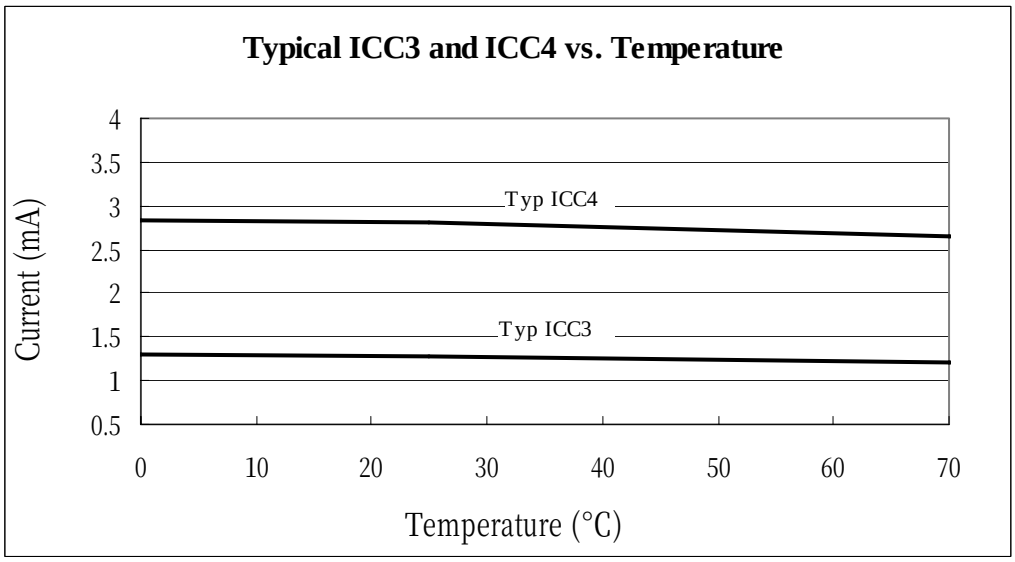


Fig. 33 Typical operating current (ICC3 and ICC4) vs. Temperature

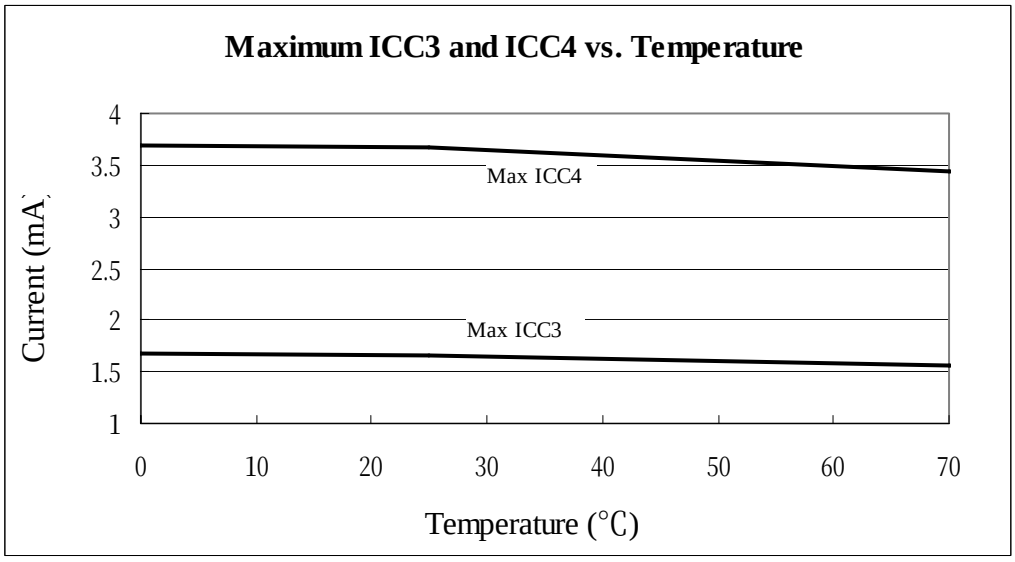


Fig. 34 Maximum operating current (ICC3 and ICC4) vs. Temperature

Two conditions exist with the Standby Current ISB1 and ISB2. These conditions are as follows:

ISB1: VDD=5V, WDT disable

ISB2: VDD=5V, WDT enable

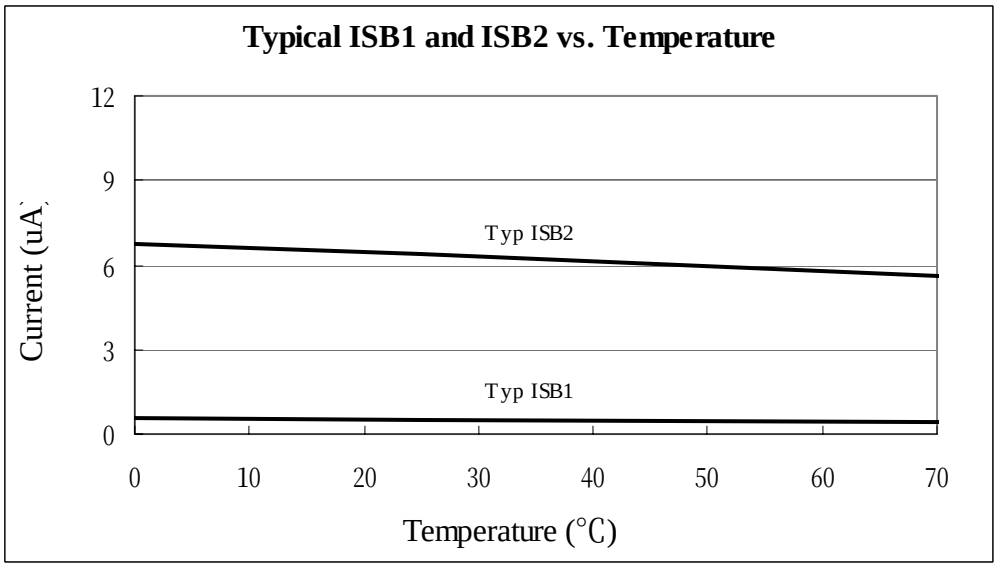


Fig. 35 Typical standby current (ISB1 and ISB2) vs. Temperature

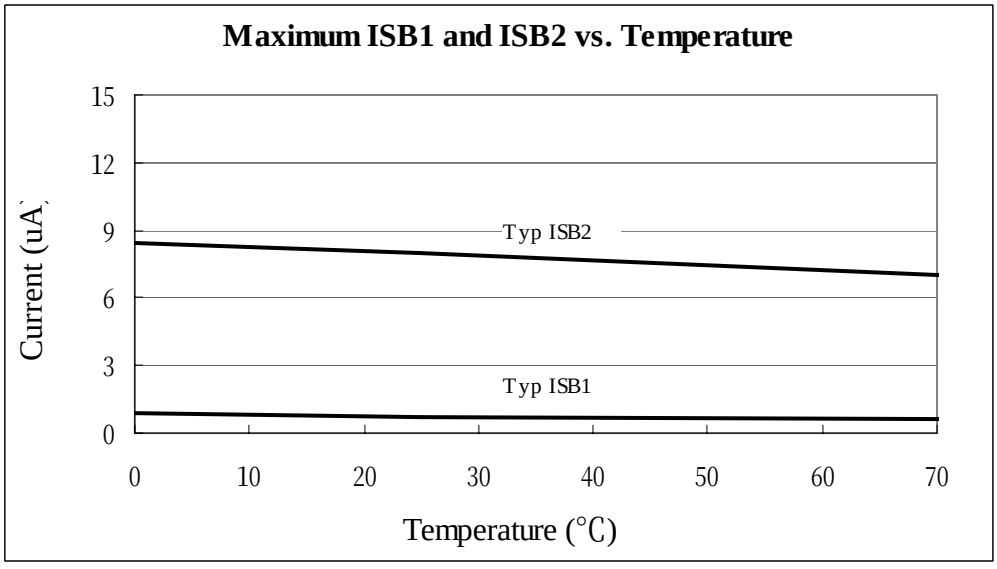


Fig. 36 Maximum standby current (ISB1 and ISB2) vs. Temperature

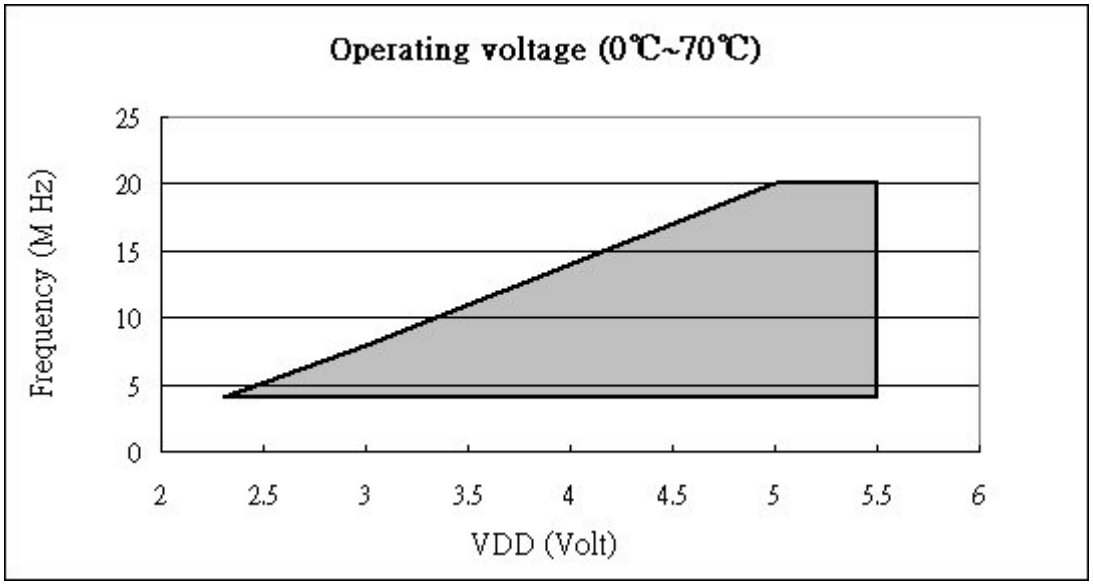


Fig. 37 Operating voltage under temperature range of 0℃ to 70℃

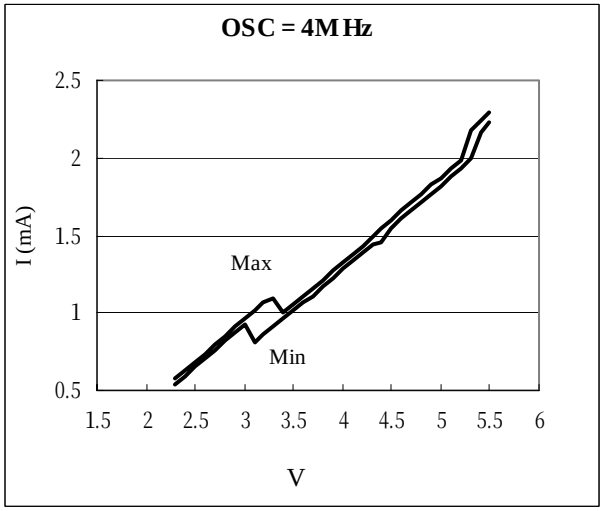


Fig. 38 V-I curve in operating mode, operating frequency is 4M Hz

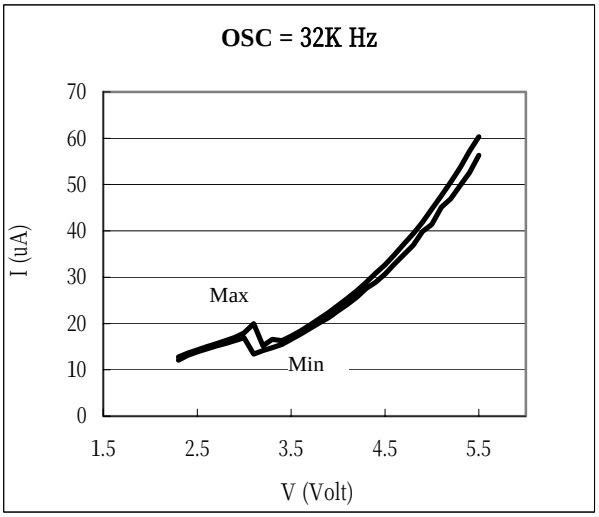


Fig. 39 V-I curve in operating mode, operating frequency is 32K Hz

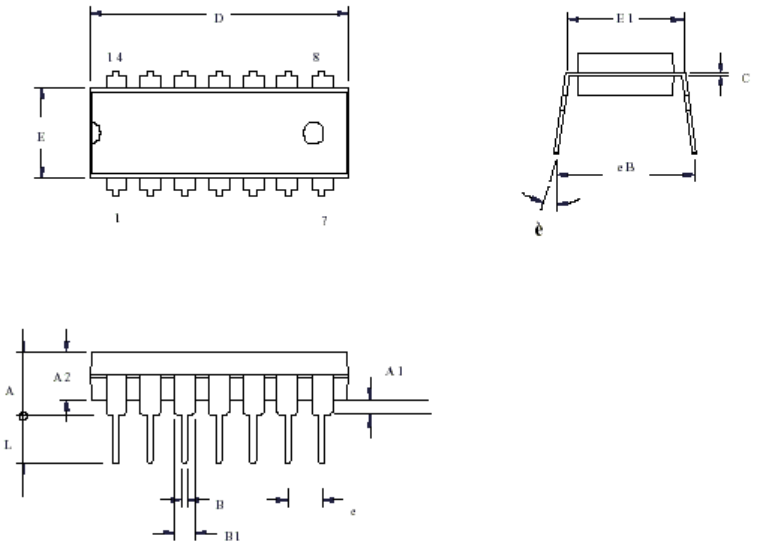
Appendix

Package Types:

OTP MCU	Package Type	Pin Count	Package Size
EM78P153SP	DIP	14	300 mil
EM78P153SN	SOP	14	150 mil

Package Information

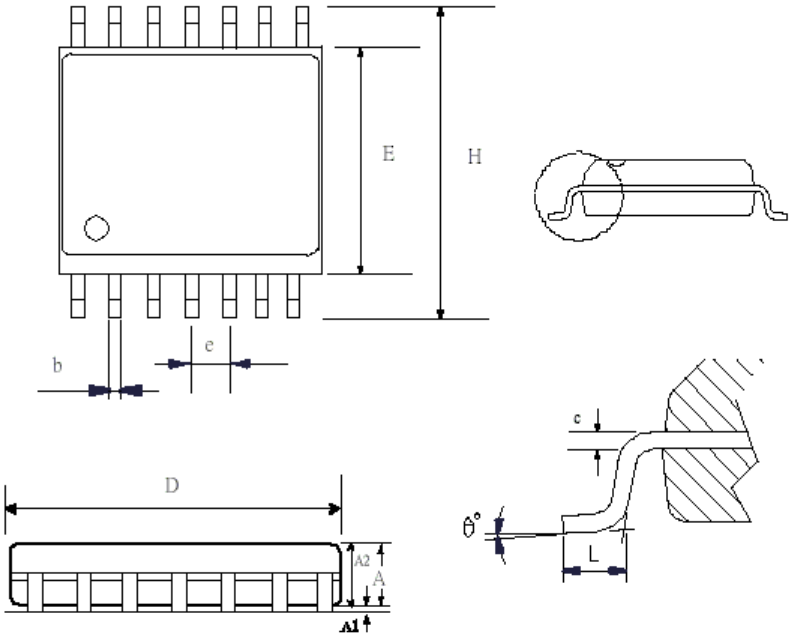
14-Lead Plastic Dual in line (PDIP) — 300 mil



Symbal	Min	Normal	Max
A			4.318
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	18.796	19.050	19.304
E	6.174	6.401	6.628
E1	7.366	7.696	8.025
eB	8.409	9.017	9.625
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(TYP)		
θ	0		15

TITLE: PDIP-14L 300MIL PACKAGE OUTLINE DIMENSION	
File : D14	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

14-Lead Plastic Small Outline (SOP) — 150 mil



Symbal	Min	Normal	Max
A	1.350		1.750
A1	0.100		0.250
b	0.330		0.510
c	0.190		0.250
E	3.800		4.000
H	5.800		6.200
D	8.550		8.750
L	0.600		1.270
e	1.27(TYP)		
θ°	0		8

TITLE: SOP-14L(150MIL) PACKAGE OUTLINE DIMENSION	
File : NSO14	Edition: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

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